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Arriagada et al.

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(45) **Date of Patent: *Jun. 23, 2015**

(54) **TRAP RICH LAYER FORMATION TECHNIQUES FOR SEMICONDUCTOR DEVICES**

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This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/013,000**

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 21/30 (2006.01)
H01L 21/02 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 21/02365*** (2013.01); ***H01L 21/2007*** (2013.01); ***H01L 21/84*** (2013.01); ***H01L 29/7803*** (2013.01); ***H01L 27/1203*** (2013.01)

(58) **Field of Classification Search**
CPC .. H01L 21/30; H01L 21/2007; H01L 29/7803
USPC 438/455–458
See application file for complete search history.

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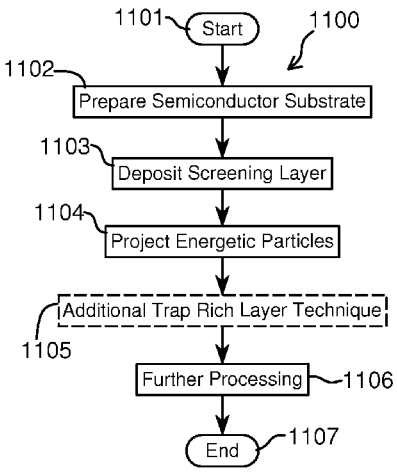
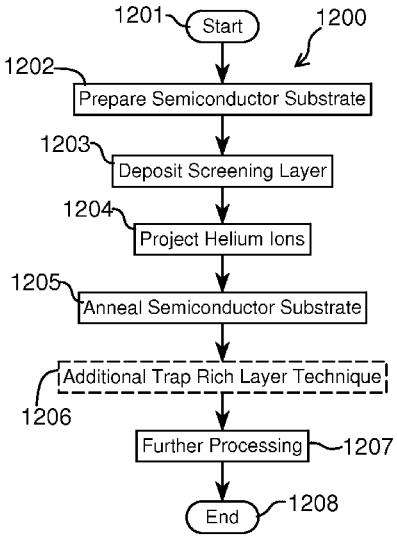
(57) **ABSTRACT**

A trap rich layer for an integrated circuit chip is formed by chemical etching and/or laser texturing of a surface of a semiconductor layer. In some embodiments, a trap rich layer is formed by a technique selected from the group of techniques consisting of laser texturing, chemical etch, irradiation, nanocavity formation, porous Si-etch, semi-insulating polysilicon, thermal stress relief and mechanical texturing. Additionally, combinations of two or more of these techniques may be used to form a trap rich layer.

22 Claims, 13 Drawing Sheets





(51) **Int. Cl.**

H01L 21/20	(2006.01)
H01L 21/84	(2006.01)
H01L 29/78	(2006.01)
H01L 27/12	(2006.01)

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2012/0146193	A1	6/2012	Stuber et al.	
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FIG. 1
Prior Art

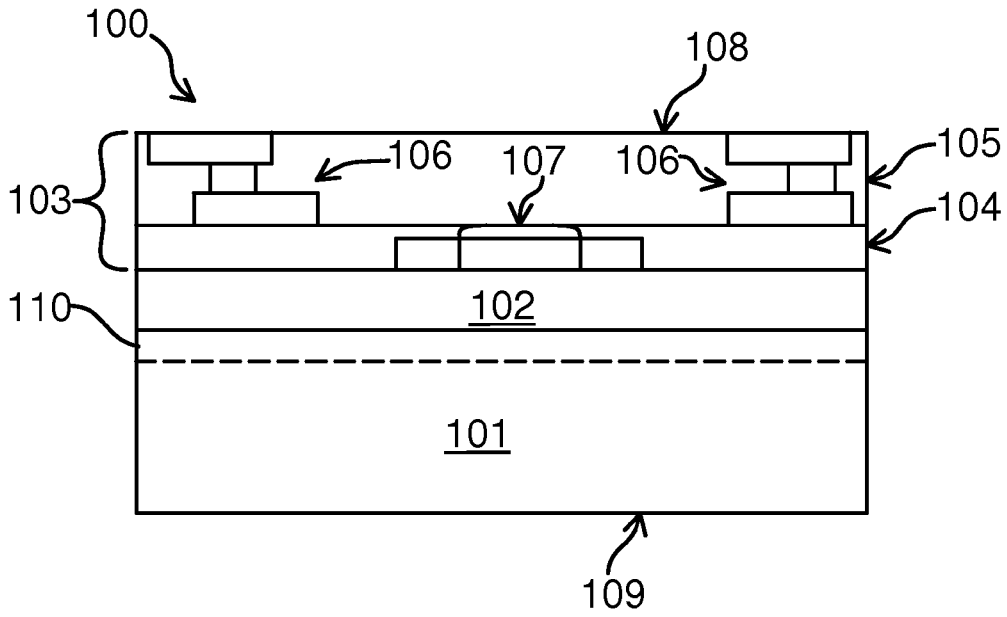

FIG. 2

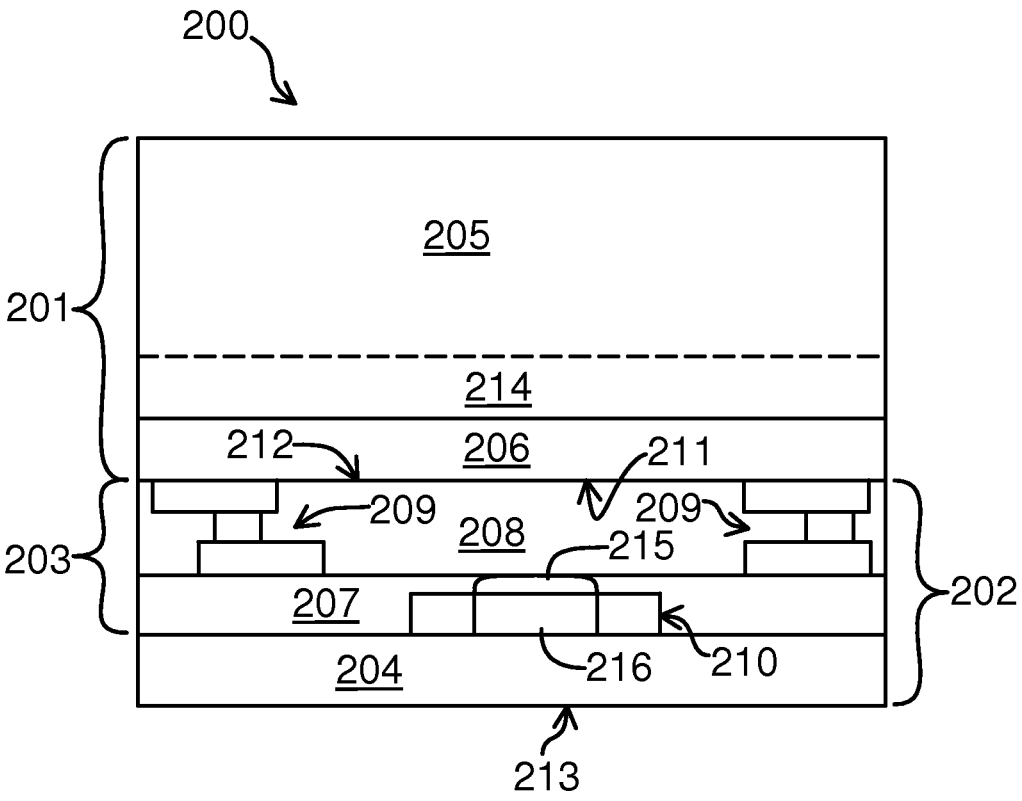
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FIG. 3

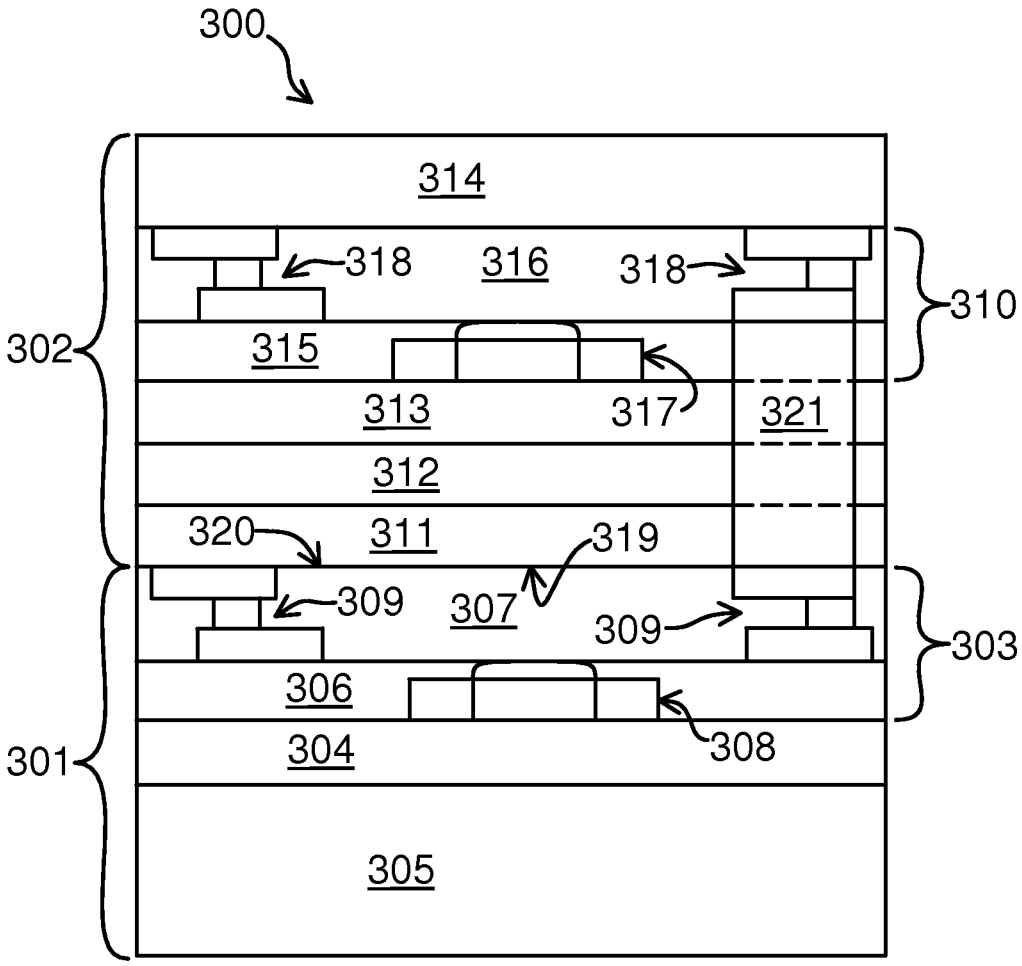
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FIG. 4

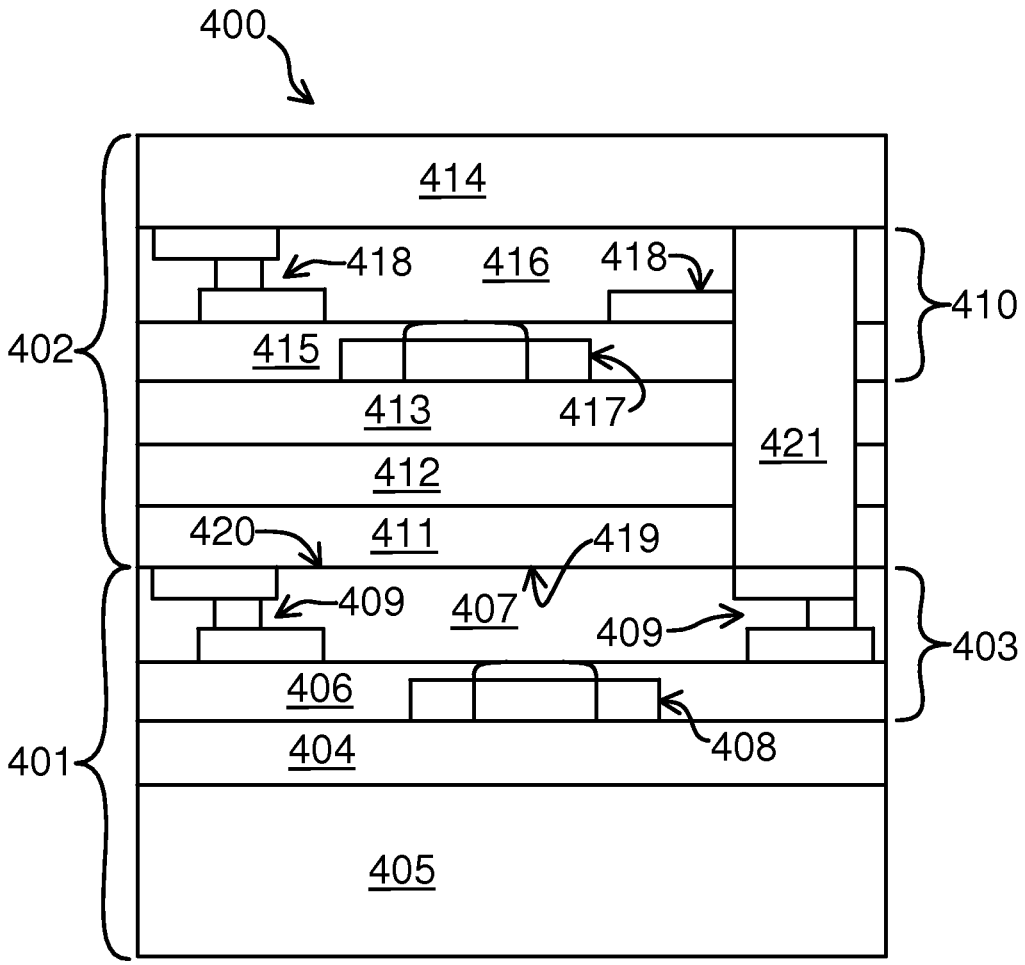
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FIG. 5

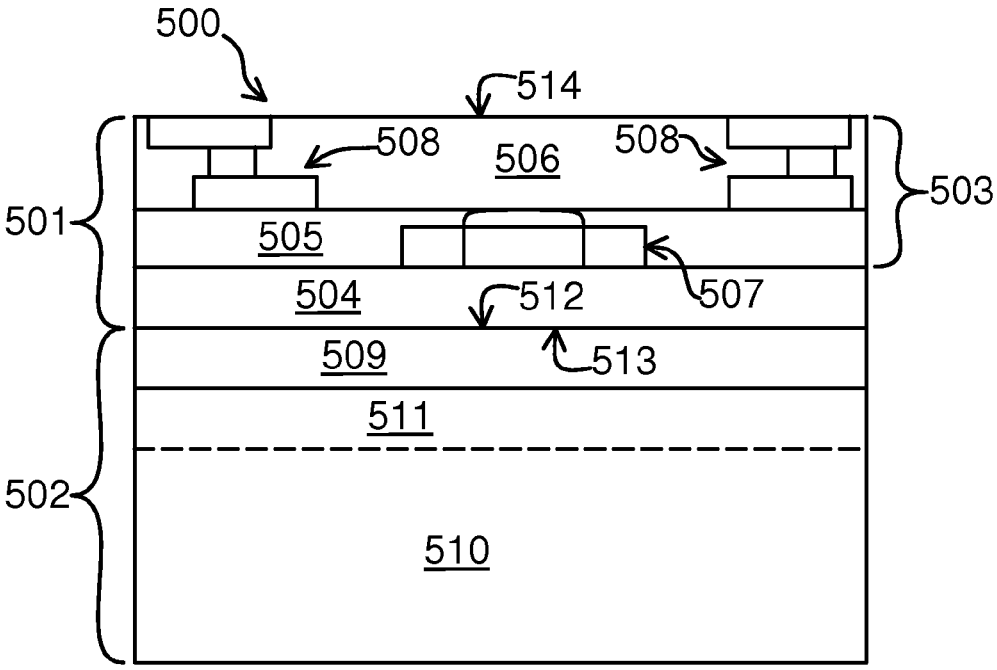


FIG. 6

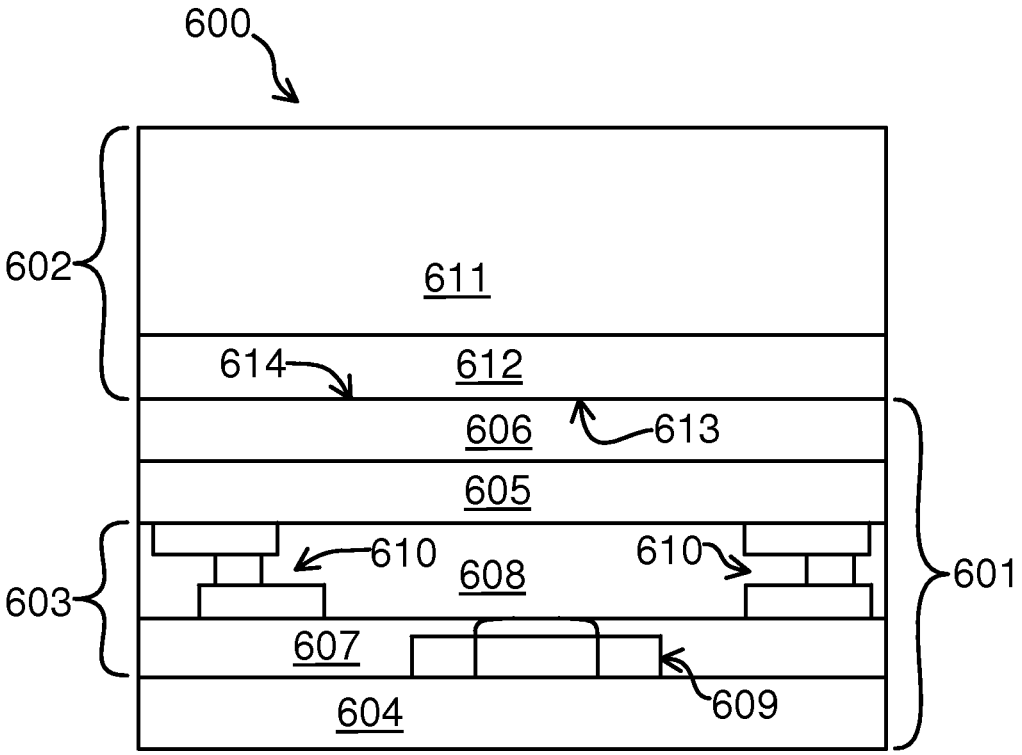


FIG. 7

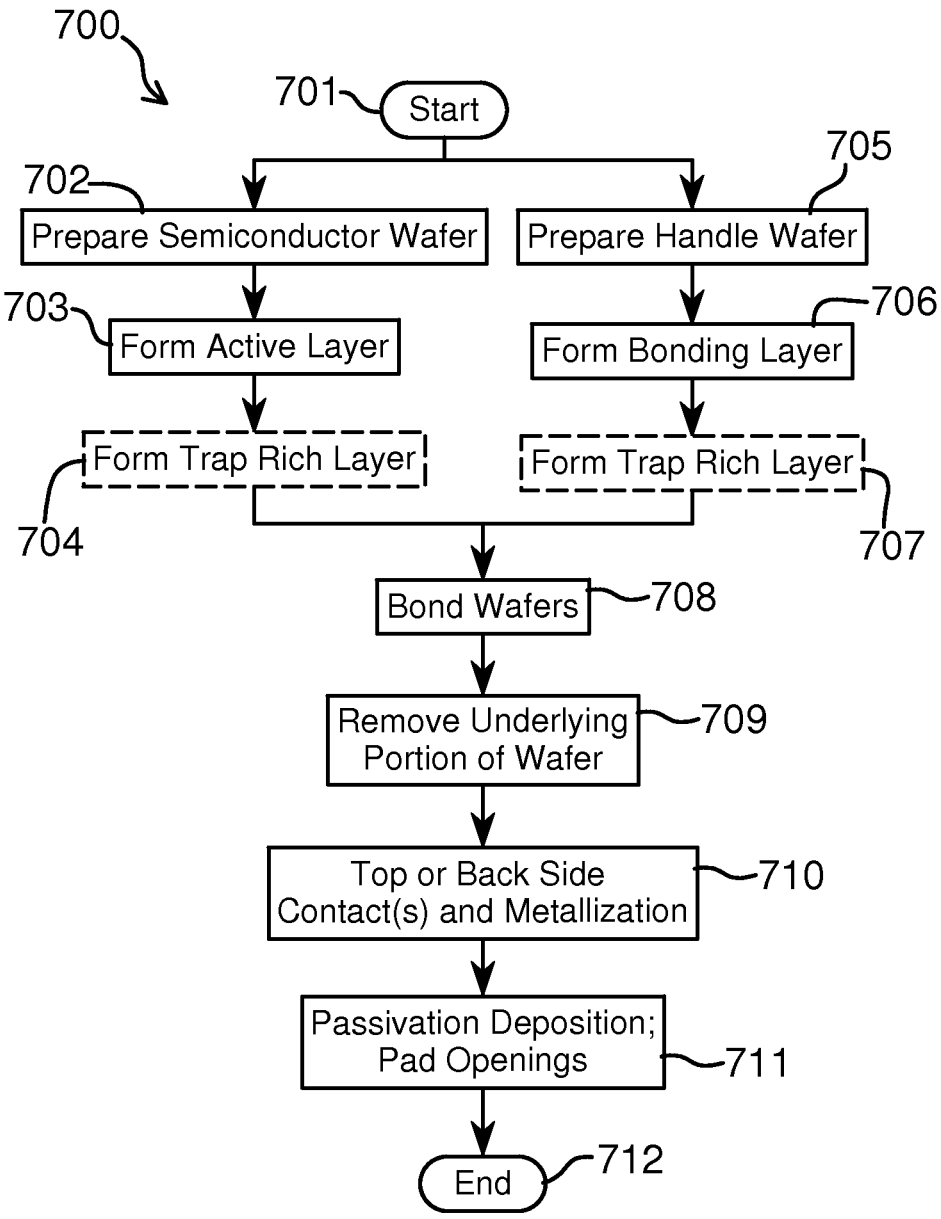

700
701
Start
705
702
Prepare Semiconductor Wafer
Prepare Handle Wafer
703
706
Form Active Layer
Form Bonding Layer
Form Trap Rich Layer
Form Trap Rich Layer
704
707
Bond Wafers
708
Remove Underlying Portion of Wafer
709
Top or Back Side Contact(s) and Metallization
710
Passivation Deposition; Pad Openings
711
End
712

FIG. 8

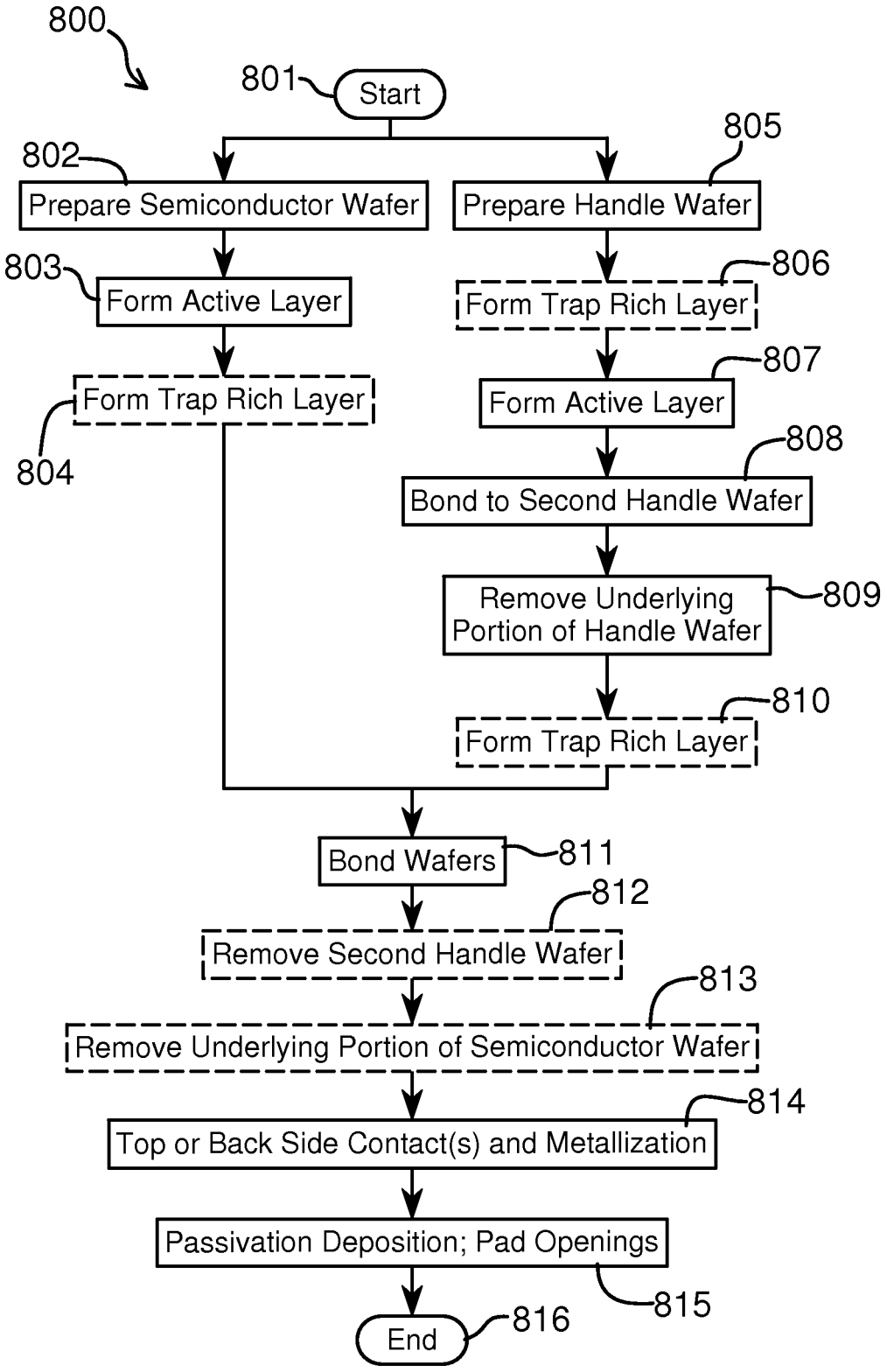

800
801
Start
802
Prepare Semiconductor Wafer
805
Prepare Handle Wafer
803
Form Active Layer
806
Form Trap Rich Layer
804
Form Trap Rich Layer
807
Form Active Layer
808
Bond to Second Handle Wafer
809
Remove Underlying Portion of Handle Wafer
810
Form Trap Rich Layer
811
Bond Wafers
812
Remove Second Handle Wafer
813
Remove Underlying Portion of Semiconductor Wafer
814
Top or Back Side Contact(s) and Metallization
815
Passivation Deposition; Pad Openings
816
End

FIG. 9

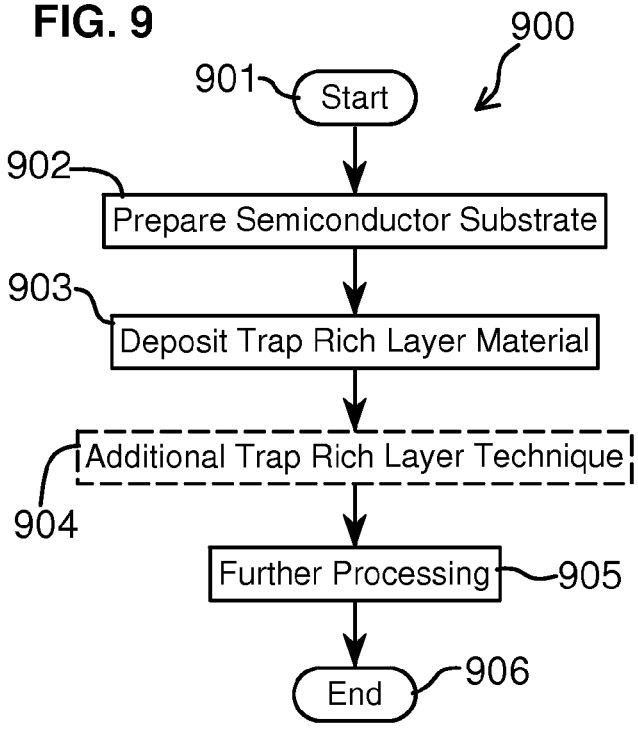

900
901
Start
902
Prepare Semiconductor Substrate
903
Deposit Trap Rich Layer Material
Additional Trap Rich Layer Technique
904
Further Processing
905
End
906

FIG. 10

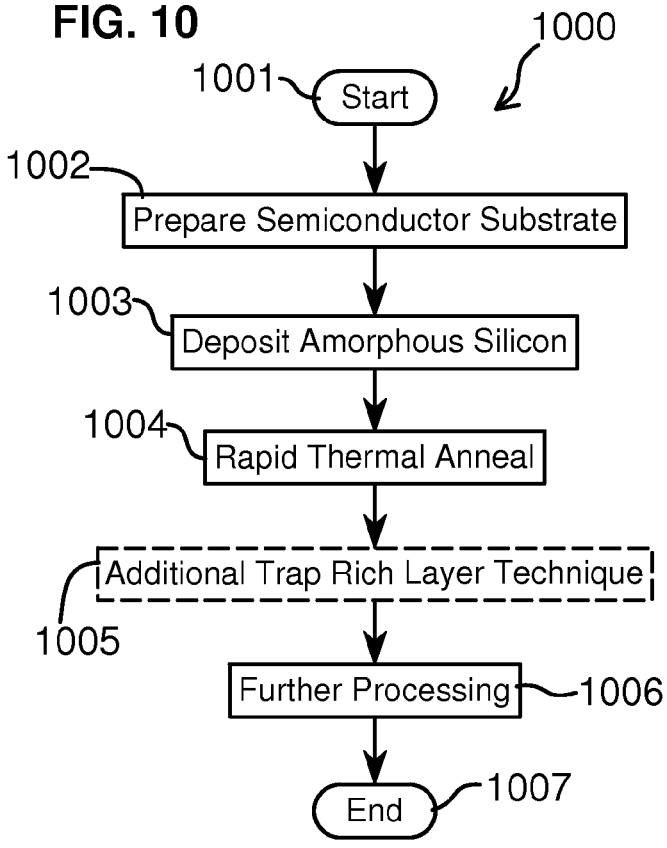

1000
1001
Start
1002
Prepare Semiconductor Substrate
1003
Deposit Amorphous Silicon
1004
Rapid Thermal Anneal
Additional Trap Rich Layer Technique
1005
Further Processing
1006
End
1007

FIG. 11

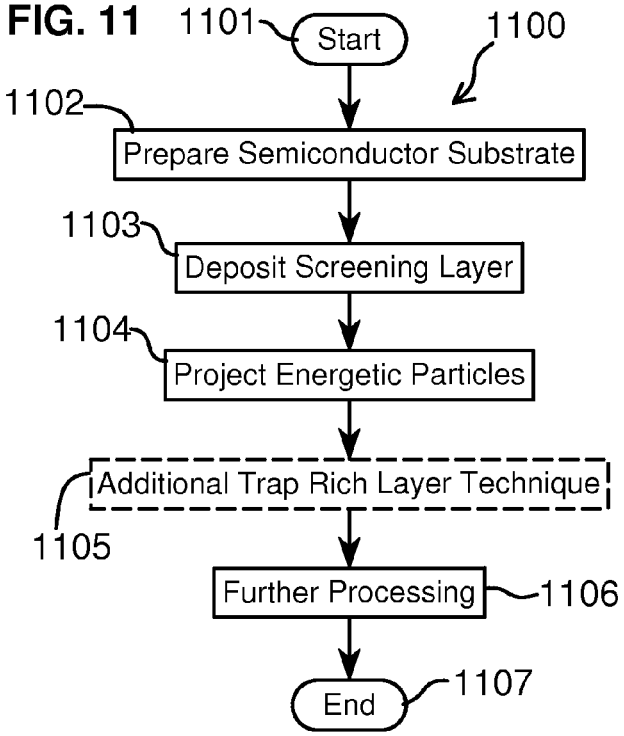

1101
Start
1100
1102
Prepare Semiconductor Substrate
1103
Deposit Screening Layer
1104
Project Energetic Particles
Additional Trap Rich Layer Technique
1105
Further Processing
1106
End
1107

FIG. 12

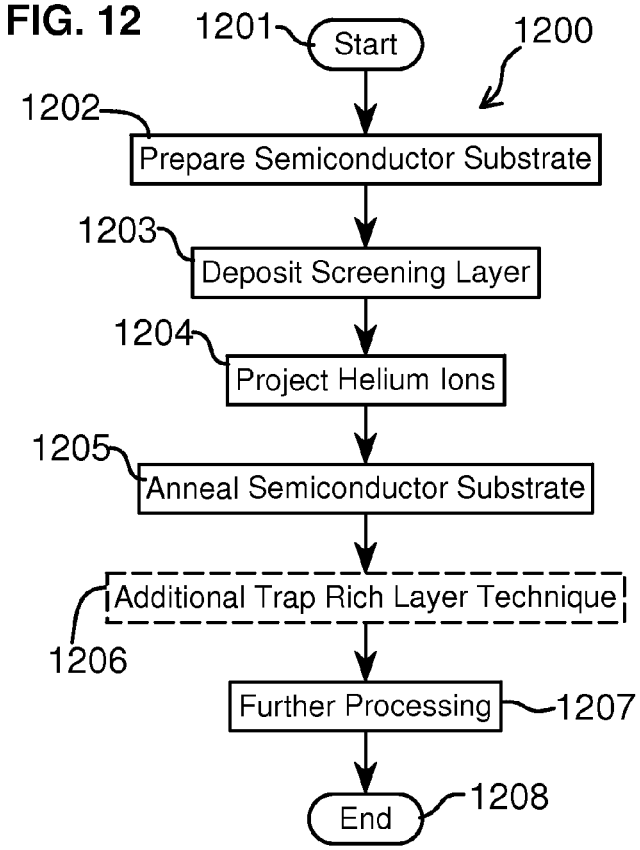

1201
Start
1200
1202
Prepare Semiconductor Substrate
1203
Deposit Screening Layer
1204
Project Helium Ions
1205
Anneal Semiconductor Substrate
Additional Trap Rich Layer Technique
1206
Further Processing
1207
End
1208

FIG. 13

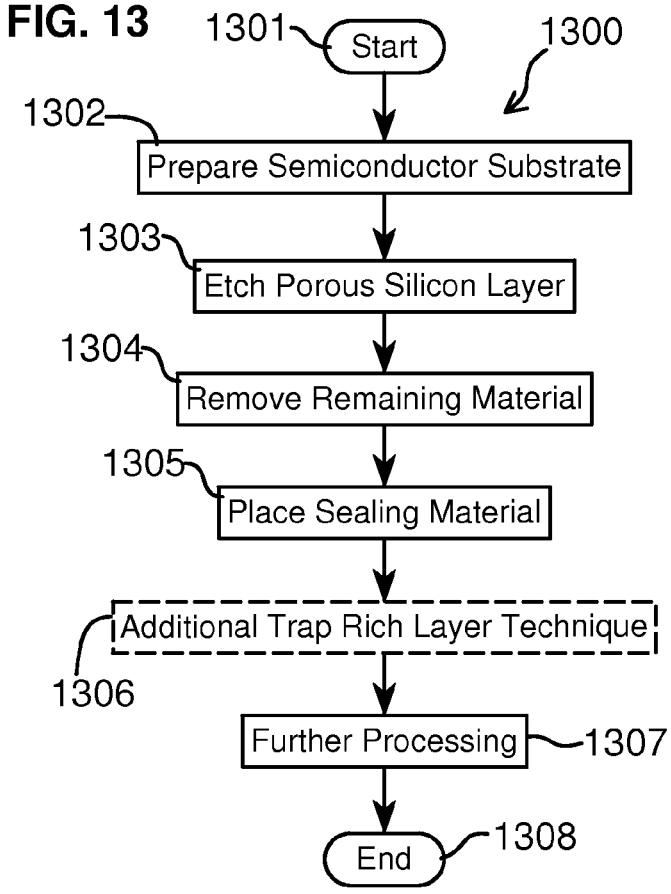

1301
Start
1300
1302
Prepare Semiconductor Substrate
1303
Etch Porous Silicon Layer
1304
Remove Remaining Material
1305
Place Sealing Material
Additional Trap Rich Layer Technique
1306
Further Processing
1307
End
1308

FIG. 14

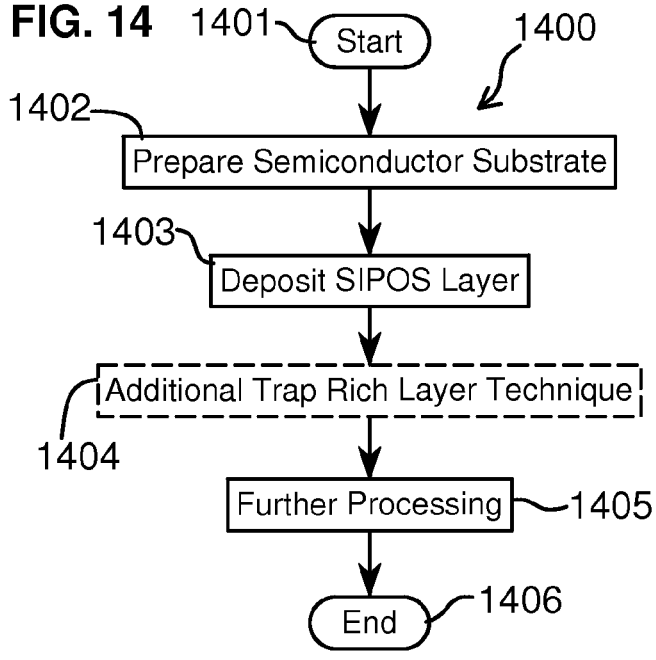

1401
Start
1400
1402
Prepare Semiconductor Substrate
1403
Deposit SIPOS Layer
Additional Trap Rich Layer Technique
1404
Further Processing
1405
End
1406

FIG. 15

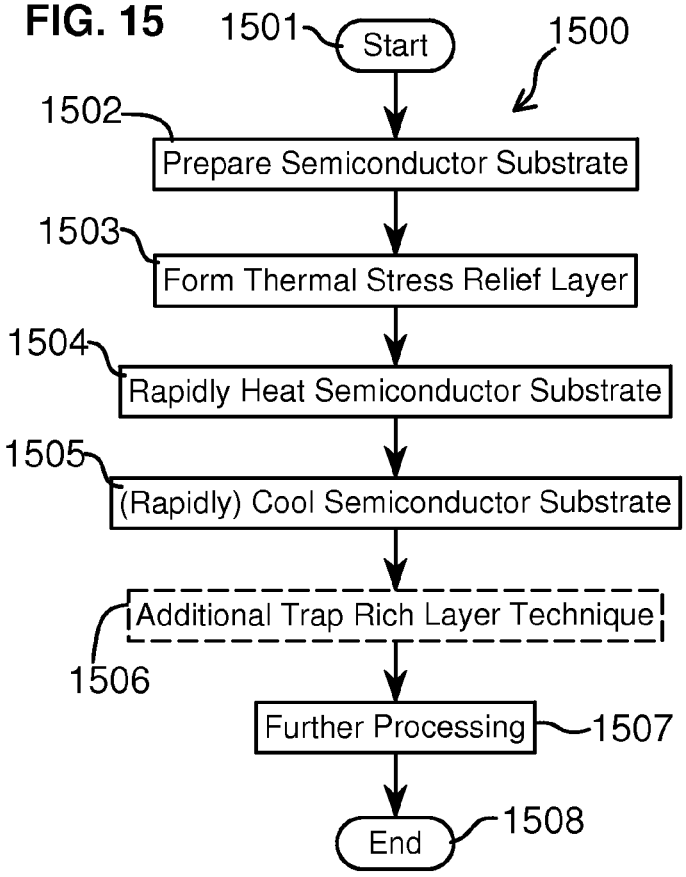

1501
Start
1500
1502
Prepare Semiconductor Substrate
1503
Form Thermal Stress Relief Layer
1504
Rapidly Heat Semiconductor Substrate
1505
(Rapidly) Cool Semiconductor Substrate
Additional Trap Rich Layer Technique
1506
Further Processing
1507
End
1508

FIG. 16

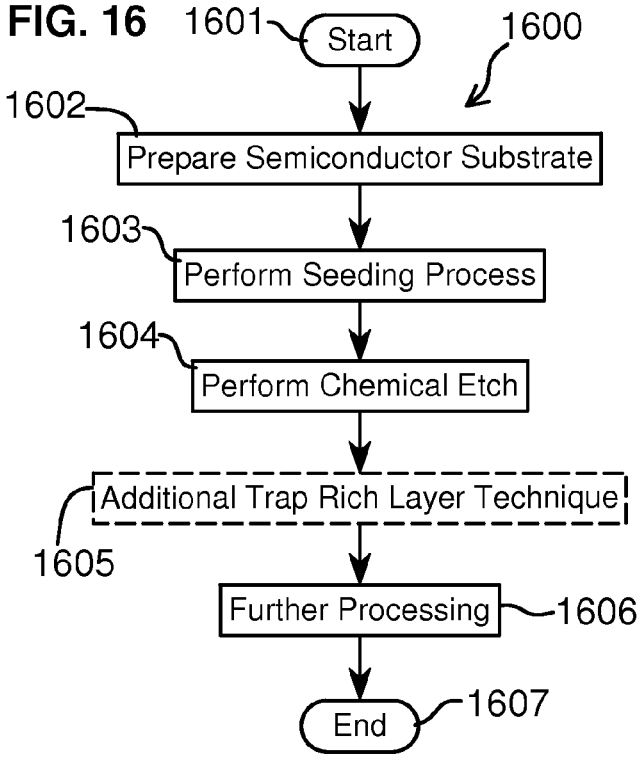

1601
Start
1600
1602
Prepare Semiconductor Substrate
1603
Perform Seeding Process
1604
Perform Chemical Etch
Additional Trap Rich Layer Technique
1605
Further Processing
1606
End
1607

FIG. 17

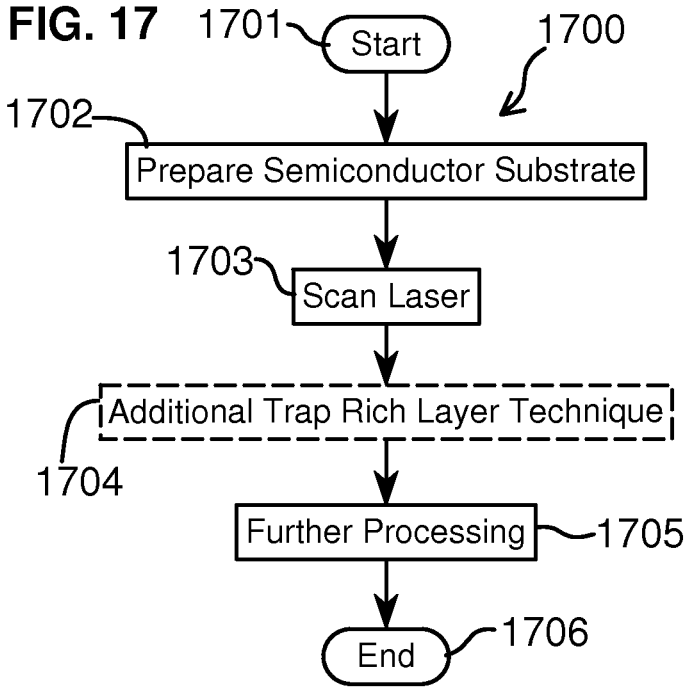
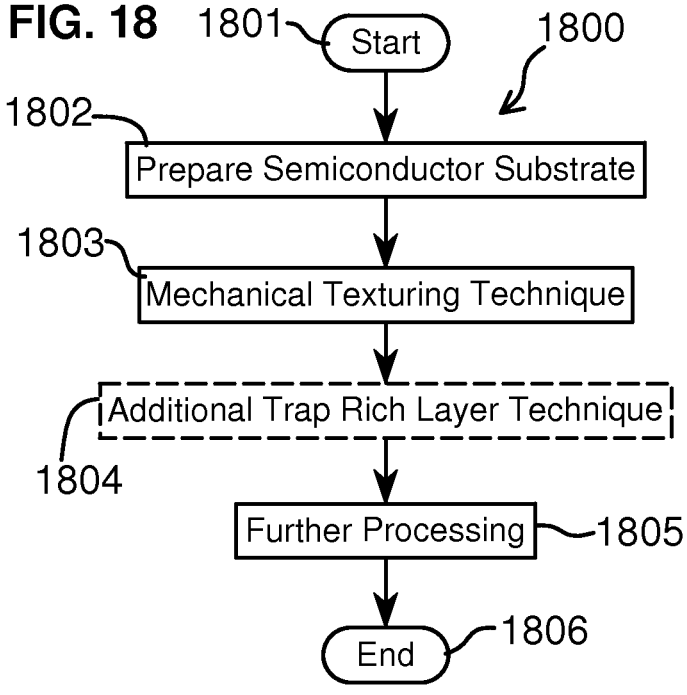

1701
Start
1700
1702
Prepare Semiconductor Substrate
1703
Scan Laser
Additional Trap Rich Layer Technique
1704
Further Processing
1705
End
1706

FIG. 18


1801
Start
1800
1802
Prepare Semiconductor Substrate
1803
Mechanical Texturing Technique
Additional Trap Rich Layer Technique
1804
Further Processing
1805
End
1806

TRAP RICH LAYER FORMATION TECHNIQUES FOR SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent is a continuation of U.S. patent application Ser. No. 13/684,623 filed Nov. 26, 2012, which is a continuation-in-part of U.S. patent application Ser. No. 13/313,231 filed Dec. 7, 2011, which claims the benefit of U.S. Provisional Patent Application No. 61/427,167 filed Dec. 24, 2010, all of which are incorporated herein by reference in their entirety. This patent application is also related to U.S. patent application Ser. No. 13/652,240 filed Oct. 15, 2012, which is a continuation-in-part of patent application Ser. No. 13/313,231. U.S. patent application Ser. No. 13/652,240 is also incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Semiconductor-on-insulator (SOI) technology, which represents an advance over traditional bulk silicon processes, was first commercialized in the late 1990s. The defining characteristic of SOI technology is that the semiconductor region in which circuitry is formed is isolated from the bulk substrate by an electrically insulating layer. One advantage of isolating circuitry from the bulk substrate is a dramatic decrease in parasitic capacitance which allows access to a more desirable power-speed performance horizon. Therefore, SOI structures are particularly appealing for high frequency applications such as radio frequency (RF) communication circuits. As consumer demand continues to tighten the power constraints faced by RF communication circuits, SOI technology continues to grow in importance.

A typical SOI structure **100** is shown in FIG. **1**. The SOI structure **100** includes a substrate layer **101**, an insulator layer **102**, and an active layer **103**. The substrate layer **101** is typically a semiconductor material such as silicon. The insulator layer **102** is a dielectric which is often silicon dioxide formed through the oxidation of the substrate layer **101** in situations where the substrate layer **101** is silicon. The active layer **103** includes an active device layer **104** and a metallization or metal interconnect layer **105**, which further include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials or components that are present after circuitry has been formed therein. The circuitry may include metal wiring **106** (e.g. in the metal interconnect layer **105**); passive devices such as resistors, capacitors, and inductors; and active devices such as a transistor **107** (e.g. in the active device layer **104**).

As used herein and in the appended claims, the region in which signal processing circuitry is formed on an SOI structure is referred to as the "active layer" of the SOI structure. For example, in FIG. **1** the active layer is the active layer **103** which includes devices or components such as the transistor **107** and the metal wiring **106**. When reference is made particularly to the layer of active semiconductor material that forms the active devices themselves the term "active device layer" (e.g. **104**) is used instead. For example, in FIG. **1** the active device layer **104** is the portion of the active layer **103** that contains the transistor **107** and does not include the metal wiring **106** of the metal interconnect layer **105**.

Also as used herein and in the appended claims, the "top" of the SOI structure **100** references a top surface **108** while the "bottom" of the SOI structure **100** references a bottom surface **109**. This orientation scheme persists regardless of the relative orientation of the SOI structure **100** to other frames of reference, and the removal of layers from, or the addition of layers to the SOI structure **100**. Therefore, the active layer **103** is always "above" the insulator layer **102**. In addition, a vector originating in the center of the active layer **103** and extending towards the bottom surface **109** will always point in the direction of the "back side" of the SOI structure **100** regardless of the relative orientation of the SOI structure **100** to other frames of references, and the removal of layers from, or the addition of layers to the SOI structure **100**.

Consumer demand continues to tighten the constraints on the quality and performance of RF devices. These constraints directly affect the required linearity and precision of the signals that are produced and decoded by RF circuits. Among other requirements, signals in one portion of a circuit must be kept from affecting and degrading signals in another portion of the circuit. This effect is called cross talk. The mitigation of cross talk is of critical importance for RF communication circuits because the impedance of certain parasitic pathways within a circuit tend to reach a minimum at frequencies that are used to carry signals in RF circuits. Since these same parasitic pathways connect nodes within a circuit that carry differing signals, the problem of cross talk is especially problematic for RF applications. In addition, it is critically important for the parasitic capacitances to which the signals within a circuit may be exposed not to be signal dependent. This requirement is critical because it is difficult to calibrate out an error that is signal dependent, and such errors are inherently nonlinear.

One solution to the problem of cross talk in electronic circuits is the use of a high resistivity substrate. With reference to FIG. **1**, increasing the resistance of the substrate layer **101** reduces cross talk by maintaining the impedance of the parasitic paths through the substrate higher than the impedance would be without an increased substrate resistance. Materials used for the substrate layer **101** typically include very lightly doped silicon such that the substrate layer **101** takes on some of the characteristics of an insulator. The use of high resistivity substrates has proven capable of extending the benefit of SOI structures for RF communication circuits by roughly two orders of frequency magnitude.

Although high resistivity substrates are capable of reducing substrate loss when they are used in SOI processes, they are highly susceptible to another phenomenon called parasitic surface conduction. The problem of parasitic surface conduction and a potential solution can be explained with reference again to FIG. **1**. As mentioned previously, the typical high resistivity substrate device insulator layer **102** is silicon dioxide, and the substrate layer **101** is high resistivity silicon. The problem of parasitic surface conduction comes from the fact that the lightly doped silicon that forms the substrate layer **101** can form an inversion or accumulation region as charge carriers are affected by signal voltages in the active layer **103**. The degree to which charge carriers in the region **110** are displaced is directly altered by the signals in the active layer **103**. As a result, the capacitance of the junction between the substrate layer **101** and the active layer **103**, as seen by the active layer, depends on the electric field emanating from the active layer. This capacitance results in nonlinearity and a concomitant loss of signal purity. In addition, an electric field can invert this interface on the side of the substrate layer **101** and create a channel-like layer within the region **110** where charge can move very easily in a lateral direction despite the fact that the substrate layer **101** is highly resistive. Therefore, this effect can also lead to signal-degrading cross talk in RF communication circuits.

A solution to the problem of the undesirable creation of the channel-like layer **110** has commonly been to form a trap rich layer along the top of the substrate layer **101** within the region **110**. The presence of this trap rich layer effectively combats parasitic surface conduction because the trap rich layer significantly degrades the carrier lifetimes of the charge carriers in the region **110**. Since the carriers cannot travel far, therefore, the effective resistance of the substrate layer **101** is preserved and the capacitance as seen by the active layer **103** is not as dependent upon the signals in the active layer **103**.

A problem with the trap rich layer in region **110**, however, is that when the trap rich layer is formed prior to the subsequent processing for the formation of the structures in the active layer **103**, those later processing steps can degrade the trap rich layer. Processing of semiconductor devices and in particular the production of active devices in the active layer **103** generally involves high temperature processes conducted at temperatures from 1000° C. to 1100° C. High temperature processing of semiconductor structures acts to anneal defects in a semiconductor crystal lattice. This effect is commonly utilized to enhance the electrical properties of electrical circuits. However, contrary to usual applications, the performance of trap rich layers formed from amorphous or polycrystalline silicon crystal patterns is actually decreased when imperfections are annealed out since the number of traps is decreased.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified cross section diagram of a prior art SOI structure.

FIG. **2** is a simplified cross section diagram of a portion of a first integrated circuit (IC) chip showing example structures therein that incorporate an embodiment of the present invention.

FIG. **3** is a simplified cross section diagram of a portion of a second IC chip showing example structures therein that incorporate another embodiment of the present invention.

FIG. **4** is a simplified cross section diagram of a portion of a third IC chip showing example structures therein that incorporate another embodiment of the present invention.

FIG. **5** is a simplified cross section diagram of a portion of a fourth IC chip showing example structures therein that incorporate another embodiment of the present invention.

FIG. **6** is a simplified cross section diagram of a portion of a fifth IC chip showing example structures therein that incorporate another embodiment of the present invention.

FIG. **7** is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. **2** and **6**, according to embodiments of the present invention.

FIG. **8** is a simplified flow chart for an example process for fabricating one or more of the structures shown in FIGS. **3** and **4**, according to embodiments of the present invention.

FIGS. **9-13** are simplified flow charts for example processes for manufacturing one or more of the trap rich layers shown in FIGS. **1-6**.

FIGS. **14-18** are simplified flow charts for example processes for manufacturing one or more trap rich layers.

DETAILED DESCRIPTION OF THE INVENTION

Reference now will be made in detail to example embodiments of the disclosed invention, one or more examples of which are illustrated in the accompanying drawings. Each example is provided by way of explanation of the present technology, not as a limitation of the present technology. In fact, it will be apparent to those skilled in the art that modifications and variations can be made in the present technology without departing from the spirit and scope thereof. For instance, features illustrated or described as part of one embodiment may be used with another embodiment to yield a still further embodiment. Thus, it is intended that the present subject matter covers all such modifications and variations within the scope of the appended claims and their equivalents.

Embodiments of the present invention generally inhibit parasitic surface conduction and enhance the RF performance of devices formed in one or more active layers of IC chips. Some embodiments of the present invention achieve these beneficial results by utilizing a layer transferred structure with a trap rich layer in a handle wafer of the layer transferred structure. In some embodiments of the present invention, the substrate is moved away from the active layer to a greater degree than in traditional SOI structures, thereby reducing the effect of substrate loss. In some embodiments of the present invention, the trap rich layer is introduced after active layer processing (e.g. CMOS processing, etc.) is complete, thereby preserving the efficacy of the trap rich layer and minimizing disruption of the integrity of the overall IC chip. Some embodiments of the present invention improve the electrical performance of devices formed in the active layer, improve the efficacy of the trap rich layer for a given potential efficacy, and minimize the potential for manufacturing defects in the overall IC chip.

Some embodiments of the present invention can be described with reference to FIG. **2**. FIG. **2** illustrates a structure **200** within a portion of an IC chip. The structure **200** may be formed by wafer bonding or layer transfer techniques, as described below. Therefore, the structure **200** generally comprises a handle wafer **201** bonded to a semiconductor wafer **202**. The structure **200** can thus be referred to as a layer transfer structure. The semiconductor wafer **202** generally comprises an active layer **203** having a bottom side in contact with an insulator layer **204**. The semiconductor wafer **202** is optionally capped by another insulator layer (not shown). The handle wafer **201** generally comprises a handle substrate layer **205** and a bonding layer **206**.

The active layer **203** may be a circuit layer that generally includes an active device layer **207** and a metallization or metal interconnect layer **208**, which generally further include a combination of dopants, dielectrics, polysilicon, metal wiring, passivation, and other layers, materials and/or components that are present after circuitry has been formed therein. The circuitry may include metal wiring **209** (e.g. in the metal interconnect layer **208**); passive devices such as resistors, capacitors, and inductors; and active devices such as a transistor **210** (e.g. in the active device layer **207**). In other embodiments, the active layer **203** may be replaced with a circuit layer having Integrated Passive Devices (IPDs, a.k.a. Integrated Passive Components, IPCs) or a mix of active and passive devices. Such IPD circuit layers generally include functional blocks such as impedance matching circuits, harmonic filters, couplers and baluns and power combiners/dividers, etc. IPD circuit layers are generally fabricated using standard wafer fabrication technologies, such as thin film and photolithography processing, among others. IPD wafers can be designed as flip chip mountable or wire bondable components. Additionally, the substrates for IPD wafers usually are thin film substrates like silicon, alumina or glass. Furthermore, IPD wafers may be formed on quartz with no semiconductor material, so the wafer **202** may be an insulating wafer. Therefore, although the description herein refers to various semiconductor wafers (e.g. **202**) and active layers (e.g. **203**),

other types of wafers and circuit layers (such as insulating wafers and IPD circuit layers, etc.) may be used in place thereof, where appropriate.

The bonding layer **206** can generally be a combination of one or more insulator layers and passivation layers used to isolate and protect the active layer **203**. The bonding layer **206** may be a material used to bond a bottom exposed surface **211** of the handle wafer **201** to a top exposed surface **212** of the semiconductor wafer **202** during the wafer bonding or layer transfer procedure. In an alternative embodiment, the bonding layer **206** is added to the semiconductor wafer **202**, instead of to the handle wafer **201**, before wafer bonding or layer transfer. In some embodiments, the bonding layer **206** is formed by chemical vapor deposition (CVD) or thermal oxidation to create an oxide layer. Depending on the embodiment, as described herein, the bonding layer **206** may be formed before or after the trap rich layer **214**. If the bonding layer **206** is formed before the trap rich layer **214**, the benefit of the trap rich layer **214** will be slightly eroded due to the heat associated with forming the bonding layer **206**. However, a single CVD or thermal oxidation process will not reduce trap density as much as will full active device processing.

The semiconductor wafer **202** may be a conventional semiconductor-on-insulator (SOI) wafer (with the insulator layer **204** formed as a buried oxide or other appropriate insulator or dielectric material) or a conventional bulk semiconductor wafer (with the insulator layer **204** implanted, deposited, grown, etc. as desired). Before bonding the handle wafer **201** to the semiconductor wafer **202**, the structures of the active layer **203** are formed in or on a substrate of the semiconductor wafer **202**. After bonding, a portion of the original semiconductor substrate (not shown) below the insulator layer **204** is removed such that a back side **213** of the insulator layer **204** is exposed. Once the underlying substrate is removed, the handle wafer **201** provides the required stabilizing force necessary to protect and preserve the electrical characteristics of devices or structures in the active layer **203**. Additionally, further metallization or interconnect wiring (not shown) may extend through the insulator layer **204** and be deposited on the back side **213** of the insulator layer **204** for back side electrical connections to the components in the active layer **203**.

An advantageous aspect of the configuration described with reference to FIG. **2** is that the resulting substrate (i.e. the handle substrate layer **205**) of the structure **200** is further from the active layer **203** than in traditional SOI or bulk semiconductor structures. This feature generally results because the bonding layer **206** is thicker than the insulator layers (similar to the insulator layer **204**) of such traditional structures. Since the handle substrate layer **205** is relatively far away from the active layer **203**, the effect of parasitic pathways and nonlinear capacitance is significantly lessened.

There are multiple reasons why the bonding layer **206** can be thicker than the insulator layer **204**. For example, the insulator layer **204** is a high-quality insulator layer and the time and expense to form thick high-quality insulators is generally prohibitive. Also, the insulator layer **204** may be kept relatively thin because wafer warpage due to different thermal coefficients of expansion between the different layers in a semiconductor wafer or IC chip becomes a more pressing issue as the thickness of such an insulator layer (e.g. **204**) increases. For an insulator layer thickness in excess of about 1 micrometer (μm), this effect cannot be mitigated easily using ordinary semiconductor manufacturing techniques. Due to these and other constraints on the maximum thickness thereof, the insulator layer **204** cannot be made arbitrarily thick. Instead, a typical thickness for the insulator layer **204** may be about 0.1 to about 1 μm. On the other hand, a typical thickness for the bonding layer **206**, in accordance with some embodiments of the present invention, may be several micrometers thick.

The layer transfer structure **200** described with reference to FIG. **2** generally has fewer problems due to nonlinear substrate capacitance and substrate loss as compared to standard SOI structures. However, conventional layer transfer devices can still suffer from substrate loss due to the presence of the substrate (e.g. the handle substrate layer **205**) in the handle wafer (e.g. **201**). To increase the resistance of the structure **200** to these phenomena, a trap rich layer **214** may be provided within the handle substrate layer **205** generally adjacent the bonding layer **206** above the active layer **203**. As used herein and in the appended claims the term "trap rich layer" generally refers to a layer having a high density of electrically active carrier traps.

As illustrated in FIG. **2**, the trap rich layer **214** can be in contact with the bonding layer **206**, and the bonding layer **206** can be in contact with the active layer **203**. This configuration will effectively eliminate the effect of parasitic substrate conduction and substrate loss by inhibiting the movement of carriers that would otherwise occur at the interface of the handle substrate layer **205** and the bonding layer **206**.

In general, a higher trap density within the trap rich layer **214** leads to a greater effect of minimizing nonlinear parasitic capacitance and parasitic surface conduction. In some embodiments of the present invention, the trap rich layer **214** has a trap density of greater than 10^{11} cm^{-2} eV^{-1}. Since embodiments in which the trap rich layer **214** is formed after the processing necessary to form structures in the active layer **203** do not suffer thermal degradation of the trap rich layer **214**, these embodiments generally enable easier or more efficient methods of forming a higher trap density than is typical in the prior art.

In some embodiments, since the trap rich layer **214** is part of the handle wafer **201** that is bonded to the semiconductor wafer **202**, the trap rich layer **214** is generally added to the semiconductor wafer **202** after most or all of the structures in the active layer **203** have been formed. Consequently, unlike in the prior art described above, the processing or fabrication methods used to form the structures in the active layer **203** generally do not affect the trap rich layer **214**.

In various embodiments of the present invention, the bonding layer **206** is provided in variant forms. For example, in some embodiments, the bonding layer **206** consists of two layers of insulator material initially separately bonded to the handle wafer **201** and the semiconductor wafer **202**. In some alternative embodiments, the trap rich layer **214** may be present on the top surface of the semiconductor wafer **202** and directly bonded to the handle wafer **201**. In this case, the bonding layer **206** is completely absent. Alternatively, the trap rich layer **214** may be present on the semiconductor wafer **202** and covered by a suitable bonding layer **206**. In this case, the trap rich layer **214** is between the active layer **203** and the bonding layer **206**. In some embodiments, the bonding layer **206** comprises silicon dioxide or any other appropriate type of insulator. In other embodiments, the bonding layer **206** comprises passivation layers and/or other auxiliary layers.

In various embodiments of the present invention, the active layer **203** can be provided in variant forms. In some embodiments, the active layer **203** contains one or more of the transistor **210**, e.g. various appropriate combinations of metal oxide semiconductor (MOS) devices, bipolar devices, vertical diffused MOS (VDMOS) power devices, etc. Various forms of the transistor **210** generally comprise a gate region **215** and a body/channel region **216**. In some embodiments of

the present invention, the gate region **215** is between the body/channel region **216** and the trap rich layer **214**. Also, in some embodiments of the present invention, the metal wiring **209** of the metal interconnect layer **208** is between the body/channel region **216** and the trap rich layer **214**. These embodiments generally exhibit an advantageous characteristic in that the active device material forming the source, drain, and channel of the active devices in the active device layer **207** (e.g. the transistor **210**) is further separated from the handle substrate layer **205** (compared to the active device layer **104** and the substrate layer **101** of FIG. **1**), thereby improving the RF performance of the active devices as described above.

The previously described advantageous characteristic is enhanced in embodiments where the active device layer **207** is at the bottom of the active layer **203** and the active regions are contacted only by the lowest layer of metal in the metal interconnect layer **208**. In other embodiments of the present invention, part or all of the metal interconnect layer **208** is added below the insulator layer **204**, e.g. after the original underlying substrate material of the semiconductor wafer **202** is removed or thinned. In this case, the active device layer **207** is not as far separated from the handle substrate layer **205** as in the previously described embodiment. However, the thickness of the bonding layer **206** may be chosen to ensure a greater beneficial separation between the active device layer **207** and the handle substrate layer **205** compared to the active device layer **104** and the substrate layer **101** of FIG. **1**.

In some embodiments of the present invention, the single structure **200** comprises multiple trap rich layers. For example, the structure **200** could comprise a trap rich layer below the insulator layer **204** in addition to the trap rich layer **214**. This additional trap rich layer may be formed according to the prior art described above or in accordance with embodiments described with reference to FIG. **5** below. In another example, the single structure **200** could comprise multiple active layers **203** (or active device layers **207**) that are separated by trap rich layers in addition to the overlying trap rich layer **214**. In addition to the mitigation of intra-layer cross talk as described above, these embodiments generally exhibit the additional advantageous characteristic of improving isolation between signals located in different active layers **203**. This characteristic is of particular importance in situations where passive devices such as inductors are located in one of the active layers **203** because it is desirous to provide good isolation between these devices and the active devices in the active device layer(s) **207**. The improved isolation thus formed by the trap rich layer(s) can additionally allow the passive devices to be closer to the active devices (e.g. the transistor **210**) to thereby reduce parasitic capacitance while still maintaining a given desirable degree of isolation.

Some embodiments of the present invention can be described with reference to FIG. **3**. FIG. **3** illustrates a structure **300** having multiple layers of signal processing circuitry. The structure **300** generally includes a semiconductor wafer **301** and a handle (or second semiconductor) wafer **302** bonded together by wafer bonding or layer transfer techniques.

The semiconductor wafer **301** generally includes an active layer **303**, an insulator (e.g. an oxide or other dielectric) layer **304** and a substrate layer **305**. The semiconductor wafer **301** is optionally capped by another insulator layer (not shown). The active layer **303** generally includes an active device layer **306** and a metallization or metal interconnect layer **307**. The active layer **303** thus also generally includes signal processing circuitry, such as one or more active devices (e.g. a transistor **308**) in the active device layer **306** and metal wiring **309** in the metal interconnect layer **307**.

The handle wafer **302** generally includes an active layer **310**, a bonding layer **311**, a trap rich layer **312**, and underlying and overlying insulator (e.g. an oxide or other dielectric) layers **313** and **314**. The active layer **310** generally includes an active device layer **315** and a metallization or metal interconnect layer **316**. The active layer **310** thus also generally includes signal processing circuitry, such as one or more active devices (e.g. a transistor **317**) in the active device layer **315** and metal wiring **318** in the metal interconnect layer **316**. The handle wafer **302** is, thus, a second semiconductor wafer in this embodiment.

According to various embodiments, the trap rich layer **312** is formed after the formation of one or both of the active layers **303** and **310**. Additionally, the trap rich layer **312** is interposed between the two wafers **301** and **302** on the top side of the semiconductor wafer **301**. Furthermore, the trap rich layer **312** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layer **214** (FIG. **2**), depending on the requirements of a desired configuration or implementation.

In some embodiments, the handle wafer **302** is formed from an SOI or bulk semiconductor wafer. Accordingly, in some embodiments, the trap rich layer **312** is formed within a semiconductor substrate of the handle wafer **302** prior to the formation of the active layer **310**. In this case, however, the subsequent formation of the structures in the active layer **310** may degrade the trap rich layer **312**, as mentioned above. However, the formation of the active layer **303** in the semiconductor wafer **301** generally does not affect the trap rich layer **312**, since the trap rich layer **312**, as part of the handle wafer **302**, is added to the semiconductor wafer **301** after the formation of the active layer **303**.

In other embodiments, the trap rich layer **312** is formed after the formation of the active layer **310**. For example, the trap rich layer **312** may be high resistivity material deposited onto a bottom surface of the insulator layer **313**, e.g. after an additional handle wafer (not shown) is bonded to the top of the handle wafer **302** and the underlying semiconductor substrate is removed or thinned to expose the insulator layer **313**. Alternatively, the underlying semiconductor substrate is not fully removed, and the trap rich layer **312** is formed in the remaining portion of the underlying semiconductor substrate, e.g. by implantation of high energy particles to create a damaged area in the underlying semiconductor substrate, as mentioned above. The additional handle wafer is subsequently removed either before or after the handle wafer **302** is bonded to the semiconductor wafer **301**. In variations of these embodiments, the additional handle wafer is optional or the overlying insulator layer **314** originates as part of the bonding layer used to bond the additional handle wafer to the handle wafer **302**. In each case, the formation of the active layer **303** in the semiconductor wafer **301** generally does not affect the trap rich layer **312**, since the trap rich layer **312**, as part of the handle wafer **302**, is added to the semiconductor wafer **301** after the formation of the active layer **303**. In other alternatives, the additional handle wafer remains attached to the handle wafer **302** immediately after bonding the semiconductor wafer **301** and the handle wafer **302**, and then either the additional handle wafer or the substrate layer **305** is removed or thinned.

In other alternative embodiments, the trap rich layer **312** is added to the handle wafer **302** by layer transfer techniques after the formation of the active layer **310**. (See the dual layer transfer technique described below with reference to FIG. **5**.) Thus, the trap rich layer **312** is formed as a layer in (or as the entire extent of) another handle wafer. The other handle wafer is then bonded to the handle wafer **302**, e.g. with the insulator

layer **313** (formed on either the other handle wafer or the handle wafer **302**) serving as a bonding layer. Then any unnecessary thickness of the other handle wafer is removed, leaving the trap rich layer **312** as part of the handle wafer **302**. Additionally, the bonding layer **311** may be formed in the other handle wafer along with the trap rich layer **312** before bonding the trap rich layer **302** to the handle wafer **302**, or the bonding layer **311** may be formed on the trap rich layer **312** after such bonding (and optionally after the removal of any unnecessary thickness of the other handle wafer). Some of these embodiments generally enable the use of a low cost polysilicon wafer, radiation damaging techniques or other appropriate techniques described below, to form the trap rich layer **312** in the other handle wafer. In each case, the formation of the active layer **303** in the semiconductor wafer **301** generally does not affect the trap rich layer **312**, since the trap rich layer **312**, as part of the handle wafer **302**, is added to the semiconductor wafer **301** after the formation of the active layer **303**.

In other embodiments, the trap rich layer **312** is added to the semiconductor wafer **301**, instead of to the handle wafer **302** (after the active layer **303** is formed, but before the semiconductor wafer **301** and the handle wafer **302** are bonded together). In this case, the bonding layer **311** is an insulating layer, and the insulating layer **313** is a bonding layer. Additionally, the active layer **310** may be formed before the bonding, so the formation of neither active layer **303** nor **310** affects the trap rich layer **312**.

The bonding layer **311** can generally be a combination of one or more insulator layers and passivation layers used to isolate and protect the active layers **303** and **310**. The bonding layer **311** may also be a material used to bond a bottom exposed surface **319** of the handle wafer **302** to a top exposed surface **320** of the semiconductor wafer **301** during the wafer bonding or layer transfer procedure. In some embodiments, the bonding layer **311** comprises an etch-stop layer used when removing material (e.g. part or all of an underlying substrate layer) from the handle wafer **302** as described below. In other embodiments, the bonding layer **311** comprises a substrate material of the handle wafer **302** that was not fully removed when the handle wafer **302** was prepared for bonding to the semiconductor wafer **301** as described below. In another alternative, the bonding layer **311** is added to the semiconductor wafer **301**, instead of to the handle wafer **302**, before wafer bonding or layer transfer.

In some embodiments, the signal processing circuitry in the active layer **310** of the handle wafer **302** is connected to the signal processing circuitry in the active layer **303** of the semiconductor wafer **301** through a metal-to-metal bond formed by a metal contact **321** between the metal wiring **309** and **318** in the metal interconnect layers **307** and **316**. The metal contact **321** may thus be stacked metal layers formed by conventional CMOS metallization processes. Although a connection through the trap rich layer **312** may slightly decrease its efficacy, the benefits accruing from the use of a trap rich layer as described above will still be realized by this structure **300**.

In various embodiments of the present invention, the wafers **301** and **302** that are on either side of the trap rich layer **312** may exhibit variant characteristics. In some embodiments of the present invention, the active layer **310** consists of passive devices such as inductors that are used for RF signal processing. The insulator layers **313** and **314** may be comprised of insulator material and passivation material meant to isolate the signal processing devices in the active layer **310**. Also, in some embodiments of the present invention, additional layers (e.g. additional handle wafers) having other signal processing circuitry may overlay the handle wafer **302**. Each such additional layer may also have an additional trap rich layer (e.g. similar to the trap rich layer **312**) interposed between the additional layer and the underlying remainder of the structure **300**.

Some embodiments of the present invention can be described with reference to FIG. **4**. FIG. **4** illustrates a layer transfer structure **400** generally having multiple layers of signal processing circuitry among elements **401-420** (e.g. having similar descriptions as, but not necessarily being identical to, elements **301-320**, respectively, of FIG. **3**).

The trap rich layer **412** is generally interposed between the active layers **403** and **410**, as described above with respect to elements **303**, **310** and **312**. The trap rich layer **412** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layer **214** or **312**, depending on the requirements of a desired configuration or implementation.

Additionally, the multiple layers of signal processing circuitry in FIG. **4** may be connected between the metal wiring **409** and **418** within the metal interconnect layers **407** and **416** of the stacked wafers **401** and **402**, respectively, using a through semiconductor via (TSV) connection **421**. The TSV connection **421** can be etched down through multiple layers of the stacked wafer **401** and **402** as needed, including through existing metallization, to which the TSV connection **421** can electrically connect. For example, the TSV connection **421** connects to circuitry in the active layer **410** of the handle (or second semiconductor) wafer **402** through a lateral contact (e.g. one or more portions of the metal wiring **418**) and to circuitry in the active layer **403** of the semiconductor wafer **401** through a bottom contact (e.g. one or more portions of the metal wiring **409**). The function of the lateral contact (**418**) can be implemented using metal sidewalls or platforms in the active layer **410**. The TSV connection **421** generally allows for relatively easy connection of additional active layers (e.g. of additional handle wafers) that may overlay the active layer **410** in a fashion similar to that of the handle wafer **402** overlaying the semiconductor wafer **401**, with additional trap rich layers interposed between each additional active layer and the underlying active layer.

Additionally, as before, the structure **400** may be capped by the insulator layer **414** which may help to isolate the signal processing circuitry in the active layer **410**. The insulator layer **414** may comprise layers of passivation and insulator material.

Some embodiments of the present invention can be described with reference to FIG. **5**. FIG. **5** illustrates a layer transfer structure **500** generally having a semiconductor wafer **501** bonded to a handle wafer **502**.

The semiconductor wafer **501** generally has an active layer **503** and an insulator (e.g. an oxide or other dielectric) layer **504**. The active layer **503** generally includes an active device layer **505** and a metallization or metal interconnect layer **506**. The active device layer **505** generally has various active devices **507**, such as various types of transistors. Additionally, the metal interconnect layer **506** generally has metal wiring **508**. Furthermore, an insulating cap layer (not shown) may be formed on the top of the metal interconnect layer **506**.

The handle wafer **502** generally has a bonding layer **509** and a substrate layer **510**. The substrate layer **510** may include a trap rich layer **511** therein. The trap rich layer **511** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layers **214**, **312** or **412**, as may be appropriate or allowable depending on the requirements of a desired configuration or imple-

mentation. Additionally, the trap rich layer **511** may comprise only a portion of the substrate layer **510** (as shown) or the entire substrate layer **510**.

The bonding layer **509** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the bonding layers **206**, **311** or **411**, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation. The bonding layer **509** generally bonds a top surface **512** of the handle wafer **502** to a bottom surface **513** of the semiconductor wafer **501**. As an alternative, the bonding layer **509** may be formed on the bottom surface **513** of the semiconductor wafer **501**, instead of on the handle wafer **502**.

In some embodiments, the structure **500** is formed by a dual layer transfer or wafer bonding technique. In this case, after most or all of the processing to form the structures in the active layer **503**, a temporary handle wafer (not shown) is bonded to a top surface **514** of the semiconductor wafer **501**. The temporary handle wafer generally provides structural support for the semiconductor wafer **501** so that part or all of a semiconductor layer (not shown) underlying the insulator layer **504** can be removed. Then the handle wafer **502** is bonded to the bottom surface **513** of the semiconductor wafer **501**, and part or all of the temporary handle wafer is removed. Any remaining part of the temporary handle wafer may, for example, form the insulating cap layer (not shown) on the top of the metal interconnect layer **506**.

The general result of embodiments in accordance with FIG. **5** is that the structure **500** bears a greater resemblance to the prior art structure **100** (FIG. **1**) than do the embodiments that accord with FIGS. **2**, **3** and **4**. This resemblance generally relates to the positioning of the trap rich layer **511** below, rather than above, the active layer **503**. However, the difference in fabrication techniques enables some advantageous differences for the structure **500** compared to the prior art structure **100**. For example, since the handle wafer **502** is bonded to the semiconductor wafer **501** after the formation of the active layer **503**, the trap rich layer **511** is generally unaffected by the formation of the structures in the active layer **503**. The trap rich layer **511** is thus generally subject to much less risk of degradation than is the prior art trap rich layer in region **110** due to any subsequent processing. Additionally, as mentioned above with respect to the insulator layer **204** and the bonding layer **206** of FIG. **2**, the bonding layer **509** can generally be made of an insulating material that is considerably thicker than the insulator layer **504**. The relatively large thickness of the bonding layer **509** generally ensures a greater beneficial separation between the active device layer **505** and the substrate layer **510** compared to that of the active device layer **104** and the substrate layer **101** of FIG. **1**. Therefore, since the substrate layer **510** is relatively far away from the active device layer **505**, the effect of parasitic pathways and nonlinear capacitance is significantly lessened compared to that of the prior art structure **100**. Additional advantages of the structure **500** may also be apparent.

In some variations on embodiments in accordance with FIG. **5**, the structure **500** is generally an intermediary structure in a process for forming the structure **300** or **400** of FIG. **3** or **4**. In this case, the substrate layer **510** is thinned or removed, and a bonding layer (e.g. **311** or **411**) is formed on a bottom surface thereof in preparation for bonding to another semiconductor wafer (e.g. **301** or **401**) having another active layer (e.g. **303** or **403**). The active layer **503** is thus either active layer **310** or **410**. Additionally, the trap rich layer **511** is thus either trap rich layer **312** or **412** and is formed after the active layers **303** and **310** or **403** and **410**. The trap rich layer **511** is thus unaffected by the formation of either active layer **303** and **310** or **403** and **410**.

In the prior art, an attempt has been made to form devices and material layers in a wafer, attach a support on top of the wafer, remove or thin portions of the wafer that underlie the devices and material layers, bond a substrate to the bottom of the wafer, and remove the top mounted support. The bottom mounted substrate has an insulator layer (such as silicon nitride or silicon oxide) on its bonding surface and comprises Au, Ag, or Li doped silicon that forms a high resistivity silicon substrate with deep level trapping sites under the insulator layer. However, the techniques described herein for forming the trap rich layer **511** generally produce a significantly higher trap density than is possible with this prior art technique. Therefore, embodiments in accordance with FIG. **5** have this significant advantage over this prior art technique. Also, Au, Ag and Li are generally considered harmful contaminants in almost all semiconductor fabrication facilities. Therefore, it is generally undesirable for wafers doped with these elements to be processed in most facilities due to concerns with cross-contamination to other processes.

Some embodiments of the present invention can be described with reference to FIG. **6**. FIG. **6** illustrates a layer transfer structure **600** generally having a semiconductor wafer **601** bonded to a handle wafer **602**.

The semiconductor wafer **601** generally has an active layer **603**, underlying and overlying insulator (e.g. an oxide or other dielectric) layers **604** and **605** and a trap rich layer **606**. The active layer **603** generally includes an active device layer **607** and a metallization or metal interconnect layer **608**. The active device layer **607** generally has various active devices **609**, such as various types of transistors. Additionally, the metal interconnect layer **608** generally has metal wiring **609**. Furthermore, an insulating cap layer (not shown) may be formed on the top of the trap rich layer **606**. The trap rich layer **606** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the trap rich layers **214**, **312**, **412** or **511**, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation.

The handle wafer **602** generally has a substrate layer **611** and a bonding layer **612**. The bonding layer **612** may have any one or more of the characteristics and may be formed by any of the techniques described herein for the bonding layers **206**, **311**, **411** or **509**, as may be appropriate or allowable depending on the requirements of a desired configuration or implementation. The bonding layer **612** generally bonds a bottom surface **613** of the handle wafer **602** to a top surface **614** of the semiconductor wafer **601**. As an alternative, the bonding layer **612** may be formed on the top surface **614** of the semiconductor wafer **601**, instead of on the handle wafer **602**.

The trap rich layer **606** is generally between the active layer **603** of the semiconductor wafer **601** and the substrate layer **611** of the handle wafer **602**. Additionally, the trap rich layer **606** is formed after most or all of the structures of the active layer **603**, so the trap rich layer **606** is generally unaffected by the formation of the structures in the active layer **603**. Therefore, even though the trap rich layer **606** is formed on the semiconductor wafer **601**, rather than on the handle wafer **602**, the trap rich layer **606** is generally subject to much less risk of degradation than is the prior art trap rich layer in region **110** due to any subsequent processing.

FIG. **7** shows a flowchart for a process **700** for fabricating at least part of an integrated circuit chip (e.g. similar to structure **200** or **600**, FIG. **2** or **6**), according to some embodiments of the present invention. It is understood, however, that the

specific process **700** is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

Upon starting (at **701**), the semiconductor wafer **202** or **601** is prepared at **702**. If the semiconductor wafer **202** or **601** is an SOI wafer, then the preparation (at **702**) may simply be to provide a standard SOI wafer. If the semiconductor wafer **202** or **601** is a bulk semiconductor wafer, then the preparation (at **702**) may include creating a buried P+ layer in the bulk semiconductor wafer **202** or **601**, e.g. by epitaxial growth or ion implantation methods. Epitaxial methods may involve epitaxially depositing a layer of P+ material on a P- or N-substrate. Then a layer of lightly-doped silicon may be epitaxially deposited to use as an active device layer. This layer may be thick enough so that up-diffusion from the P+ layer does not reach the active device layer **207** or **607** by the end of processing to form the structures in the active layer **203** or **603**. Ion implantation methods, on the other hand, may involve performing a high-dose, high-energy ion (e.g. Boron, etc.) implant into the surface of the bulk semiconductor wafer, forming a buried P+ layer deep enough so it will not diffuse up to the active device layer **207** or **607** during processing to form the structures in the active layer **203** or **603**.

At **703**, the active layer **203** or **603** is formed to produce a circuit with a set of active devices in the semiconductor wafer **202** or **601**. For an SOI wafer, the active layer **203** or **603** may be manufactured using a standard SOI process. For a bulk semiconductor wafer, the active layer **203** or **603** may be formed with a process that provides an etch stop for a subsequent substrate removal, such as the aforementioned P+ layer formed below the active device layer. Additionally, a chemical mechanical polishing is optionally performed of the top surface of the semiconductor wafer **202** or **601**.

For embodiments according to FIG. **6**, the trap rich layer **606** is formed (at **704**) on the semiconductor wafer **601** above, and after the formation of, the active layer **603**. Additionally, the insulator (e.g. an oxide or other dielectric) layer **605** may be formed beforehand. Also, an additional dielectric/oxide layer (not shown) may be formed over the trap rich layer **606**. The trap rich layer **606**, the insulator layer **605** and the additional dielectric/oxide layer may be deposited or epitaxially grown above the active layer **603** or added by layer transfer techniques from another handle wafer. If the trap rich layer **606** is added by layer transfer techniques, then the other handle wafer is processed separately to form the trap rich layer **606** and any adjacent dielectric or insulator layers. In this case, for example, the trap rich layer **606** may be polycrystalline semiconductor on dielectric on substrate or damaged single crystal top semiconductor on dielectric on substrate. After bonding the other handle wafer to the semiconductor wafer **601**, the substrate of the other handle wafer may be removed, e.g. as described herein for removing semiconductor substrate material. The dielectric layer that was under the trap-rich layer **606** is optionally left in place. Additionally, another dielectric layer is optionally deposited on the top surface exposed after removing the semiconductor substrate of the other handle wafer.

If direct bonding is subsequently to be performed to bond the semiconductor wafer **202** or **601** to the handle wafer **201** or **602**, the top surface of the semiconductor wafer **202** or **601** may be planarized after **703** or **704**. On the other hand, if an adhesive bond is to be performed, then planarization may not be necessary.

Separately from **702-704**, the handle wafer **201** or **602** is prepared (at **705**). Such preparation may include the formation (at **706**) of the bonding layer **206** or **612** and, for embodiments according to FIG. **2**, the formation (at **707**) of the trap rich layer **214**, by any appropriate method or in any appropriate order as described above.

At **708**, the handle wafer **201** or **602** is bonded to the top surface of the semiconductor wafer **202** or **601**. The bonding may be a direct oxide-oxide bond, an adhesive bond, an anodic bond, a low-temperature glass frit bond, a molecular bond, an electrostatic bond, etc., as appropriate for a given situation. For embodiments according to FIG. **2**, therefore, even though the trap rich layer **214** may be formed in the handle wafer **201** at any time before, during or after the formation of the active layer **203** in the semiconductor wafer **202**, the trap rich layer **214** is not added to the structure **200** until after the formation of the active layer **203**.

At **709**, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the semiconductor wafer **202** or **601** is substantially removed or thinned. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc., leaving at least the active device layer **207** or **607** (or the insulator layer **204** or **604**, if it is part of the original semiconductor wafer **202** or **601**). For embodiments using a bulk semiconductor wafer, the original underlying substrate is removed to the P+ layer (described above) using a wet chemical etch that is highly selective to P+ material (for example EDP, KOH, or TMAH). The etch can be either chemical or electro-chemical. Additionally, the P+ layer is optionally removed using any combination of grinding, polishing, CMP, dry etch, or non-selective wet etch. The P+ layer will only be a few microns in thickness, so a much better uniformity of a remaining relatively thin (e.g. less than 1 μm) semiconductor film can be achieved than if the semiconductor wafer **202** or **601** was thinned mechanically. Furthermore, after removing/thinning the various layers or materials at **709**, a passivation dielectric layer(s) is optionally deposited on the newly-exposed surface to reduce effects due to moisture and ionic contamination ingress.

At **710**, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). At **711**, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process **700** then ends at **712**.

FIG. **8** shows a flowchart for a process **800** for fabricating at least part of an integrated circuit chip (e.g. similar to structure **300** or **400**, FIG. **3** or **4**), according to some embodiments of the present invention. It is understood, however, that the specific process **800** is shown for illustrative purposes only and that other embodiments (in addition to specifically mentioned alternative embodiments) may involve other processes or multiple processes with other individual steps or a different order or combination of steps and still be within the scope of the present invention.

Upon starting (at **801**), the semiconductor wafer **301** or **401** is prepared at **802** and the active layer **303** or **403** is formed at **803**. For example, **802** and **803** may be similar to **702** and **703**, respectively, as described above for an SOI wafer or a bulk semiconductor wafer. At this point, if an electrical connection is to be made between the semiconductor wafer **301** or **401** and the handle wafer **302** or **402** (e.g. via the metal contact

321), then the semiconductor wafer **301** or **401** has metal exposed with the metal surface coplanar with a top dielectric surface.

Optionally, the trap rich layer **312** or **412** may be formed (at **804**) on top of the semiconductor wafer **301** or **401**, similar to the formation of the trap rich layer **606** (at **704**), as described above, instead of forming the trap rich layer **312** or **412** in the handle (or second semiconductor) wafer **302** or **402**, as described below. In this case, since the active layer **303** or **403** is formed before the trap rich layer **312** or **412**, the trap rich layer **312** or **412** is unaffected by the processes that form the active layer **303** or **403**. Additionally, since the active layer **310** or **410** is formed in the handle wafer **302** or **402** before bonding to the semiconductor wafer **301** or **401**, the trap rich layer **312** or **412** is also unaffected by the processes that form the active layer **310** or **410**.

If the trap rich layer **312** or **412** is added (at **804**) by layer transfer techniques, then another handle wafer is processed separately to form the trap rich layer **312** or **412** and any adjacent dielectric or insulator layers. In this case, for example, the trap rich layer **312** or **412** may be polycrystalline semiconductor on dielectric on substrate or damaged single crystal top semiconductor on dielectric on substrate. After bonding the other handle wafer to the semiconductor wafer **301** or **401**, the substrate of the other handle wafer may be removed, e.g. as described herein for removing semiconductor substrate material. The dielectric layer that was under the trap-rich layer **312** or **412** is optionally left in place. Additionally, another dielectric layer is optionally deposited on the top surface exposed after removing the semiconductor substrate of the other handle wafer.

Separately from **802-804**, the handle wafer **302** or **402** is prepared (at **805**), e.g. similar to **702** or **802**, as described above for an SOI wafer or a bulk semiconductor wafer. If the trap rich layer **312** or **412** is not formed at **804**, then since the trap rich layer **312** or **412** is below the active layer **310** or **410**, the trap rich layer **312** or **412** may optionally be formed (at **806**) before the formation (at **807**) of the active layer **310** or **410**. Since the active layer **303** or **403** is formed in the semiconductor wafer **301** or **401** before bonding to the handle wafer **302** or **402**, the trap rich layer **312** or **412** is unaffected by the processes that form the active layer **303** or **403**. However, since the subsequent formation of the active layer **310** or **410** could degrade the trap rich layer **312** or **412**, the trap rich layer **312** or **412** may be formed from the back side of the handle wafer **302** or **402** after the formation (at **807**) of the active layer **310** or **410**, as described below at **810**.

The active layer **310** or **410** is formed at **807**. The active layer **310** or **410** may have active devices, passive devices, or both, depending on the situation or embodiment. The active layer **310** or **410** (or the handle wafer **302** or **402** as a whole) may have similar or different material layer sequences to that of the active layer **303** or **403** (or of the semiconductor wafer **301** or **401** as a whole). Additionally, the active layer **310** or **410** may be based on SOI wafer (e.g. layers including a substrate, a buried oxide and device semiconductor material) or bulk semiconductor wafer (e.g. layers including a lightly doped substrate, a semiconductor layer doped P+ at the surface and device semiconductor material) types of processes, regardless of the types of wafer or processes used to form the active layer **303** or **403**.

At **808**, a second handle wafer (not shown) is bonded to a top surface of the handle wafer **302** or **402** at least after the formation (at **807**) of the active layer **310** or **410** and optionally after the formation (at **806**) of the trap rich layer **312** or **412**. The second handle wafer may be permanent or temporary, depending on the situation or embodiment.

At **809**, the original underlying, or back side, portion (e.g. a semiconductor substrate) of the handle wafer **302** or **402** is substantially removed or thinned. In some respects, this removal may be similar to **709** above. Most of the semiconductor substrate can be removed by back side grinding. A final portion of the semiconductor substrate can be removed by a wet etch, selective chemical mechanical polishing (CMP), a dry etch, etc. If the thickness of the remaining semiconductor material is not a critical parameter, then a mechanical stop may be sufficient.

If the trap rich layer **312** or **412** (or the bonding layer **311** or **411**) has already been formed (at **806**) in the handle wafer **302** or **402**, then the removal/thinning of the underlying portion stops at this point. On the other hand, if the trap rich layer **312** or **412** is not already present, then the removal/thinning stops at least at the active device layer **315** or **415** (or the insulator layer **313** or **413**, if it is part of the original handle wafer **302** or **402**).

If the trap rich layer **312** or **412** has not been formed at **804** or **806**, then the trap rich layer **312** or **412** may be formed at **810**. In this case, since the underlying portion of the handle wafer **302** or **402** has been removed or thinned, the trap rich layer **312** or **412** can be formed on the back side of the handle wafer **302** or **402**. The trap rich layer **312** or **412** may thus be formed by any appropriate method. If the trap rich layer **312** or **412** is formed by a dual layer transfer or wafer bonding technique as described with respect to FIG. **5**, then the underlying substrate layer **510** may be removed or thinned before the handle wafer **302** or **402** is bonded to the semiconductor wafer **301** or **401**.

Additionally, in this case, since the active layer **310** or **410** is formed before the trap rich layer **312** or **412** is added to the handle wafer **302** or **402**, the trap rich layer **312** or **412** is unaffected by the processes that form the active layer **310** or **410**. Furthermore, since the active layer **303** or **403** is formed in the semiconductor wafer **301** or **401** before bonding to the handle wafer **302** or **402**, the trap rich layer **312** or **412** is also unaffected by the processes that form the active layer **303** or **403**.

Prior to bonding the handle wafer **302** or **402** and the semiconductor wafer **301** or **401**, the bonding layer **311** or **411** may be formed on the back side of the handle wafer **302** or **402** (or on the top side of the semiconductor wafer **301** or **401**). Additionally, if an electrical connection is to be made between the semiconductor wafer **301** or **401** and the handle wafer **302** or **402** (e.g. via the metal contact **321**), then the back side of the handle wafer **302** or **402** is processed to form metal surfaces coplanar with the bottom dielectric surface. The handle wafer **302** or **402** is then bonded to the semiconductor wafer **301** or **401** at **811**. If an electrical connection is to be made between the semiconductor wafer **301** or **401** and the handle wafer **302** or **402**, then bond may be metal-to-metal, as well as dielectric-to-dielectric.

At **812**, the second handle wafer may be removed from the top side of the handle wafer **302** or **402**. However, if it is desired to have back side electrical connections (e.g. solder balls, bumps, pillars, etc.) for the structure **300** or **400**, then the second handle wafer may be permanently left in place and an underlying portion of the insulator layer **305** or **405** may be removed or thinned (at **813**).

The process **800** may optionally repeat **805-812** to stack additional active layers onto the structure **300** or **400**. Each additional active layer may have a trap rich layer between it and the preceding underlying active layer. Additionally, active layers between two other active layers may have the metal contact **321** or the TSV connection **421** to electrically connect to at least one of the two other active layers.

At **814**, patterned contact and metallization are formed for any top or back side connections (e.g. top or bottom electrodes and contacts, etc., as desired). In some embodiments, material layers may also be optionally etched from the exposed top or back side surface through one of the active layers **403** or **410** to the other active layer **410** or **403**; thereby exposing metal (e.g. metal sidewalls and/or shelves) in the metal interconnect layer **407** or **416** through a deep hole or trench. The hole or trench may be filled with metal to form the TSV connection **421** to interconnect the active layers **403** and **410** together and optionally to provide an electrical connection to the active layers **403** and/or **410** from a source external to the structure **400**.

At **815**, various passivation deposition techniques are performed and pad openings are formed, so the overall IC chip can be generally completed with bumps, pillars, or other post-processing metallization. The process **800** then ends at **816**.

Some embodiments of the present invention described above exhibit an advantageous aspect in that the efficacy of the trap rich layer **214**, **312**, **412**, **511** or **606** is generally not mitigated by further semiconductor processing. As described above, in specific embodiments of the present invention the trap rich layer **214**, **312**, **412**, **511** or **606** is formed on the top surface of the semiconductor wafer **202**, **301**, **401**, **501** or **601** or is provided by the handle wafer **201**, **302**, **402**, **502** or **602** after the semiconductor wafer **202**, **301**, **401**, **501** or **601** has undergone active layer processing. By introducing the trap rich layer **214**, **312**, **412**, **511** or **606** after active layer processing is complete, the efficacy of the trap rich layer **214**, **312**, **412**, **511** or **606** is preserved to a greater degree. Although bonding processes will sometimes require increased temperatures, these processes typically only require temperatures of 200° C. to 400° C. which will have a much more benign effect on the number of traps that are present in the trap rich layer **214**, **312**, **412**, **511** or **606**.

Some embodiments of the present invention described above exhibit an advantageous aspect in that the trap rich layer **214**, **312**, **412**, **511** or **606** does not interfere with the production and composition of the insulator layer **204**, **304**, **313**, **404**, **413**, **504** or **604** and the active layer **203**, **303**, **310**, **403**, **410**, **503** or **603**. In the prior art approaches (e.g. FIG. **1**), the trap rich layer (e.g. in region **110**) is formed below the insulator layer **102** and the insulator layer **102** is then grown or deposited on top of the trap rich layer in region **110**. The uniformity of the insulator layer is of critical importance for the performance of the active devices in the active layer of the overall structure. Also, the uniformity of the insulator layer will affect the flatness of the surface of the overall structure if it is used in a layer transferred structure, and the flatness of the surface of the overall structure is important for wafer bonding. Due to the tight constraints placed on the insulator layer, the trap rich layer must also be extremely planar or other significant manufacturing processes must be employed to correct for irregularities in the insulator layer as it is formed over the trap rich layer. In addition, pin holes in the insulator layer can be disastrous in terms of their effect on the performance of devices in the active layer. The introduction of the trap rich layer at a later stage eliminates both of these concerns. First, the uniformity of the bonding layer has a much smaller effect on the performance of the circuitry in the active layer as compared to the uniformity of the insulator layer so the manufacturing process used with relation to these two layers can be significantly relaxed as compared to the prior art. In addition, if the trap rich layer causes pin holes in any insulating layer that is part of the bonding layer, they will not affect the circuit because the top surface of the semiconductor wafer is also generally covered in an insulator that will shield the circuitry located therein.

In some embodiments of the present invention, variations on the process **700** or **800** can be used to produce structures having multiple trap rich layers. Process flows used to produce a structure with multiple trap rich layers can be very similar to those described above. In some embodiments of the present invention, the process **700** or **800** can begin with the provisioning of a semiconductor wafer having a trap rich layer below the insulator layer **204**, **304**, **404** or **604**. As a result, the final layer transferred structure **200**, **300**, **400** or **600** will have a top side (or intermediate) trap rich layer **214**, **312**, **412** or **606** and a back side trap rich layer (not shown).

In various embodiments of the present invention, the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are provided in variant forms. In some embodiments, for example, the trap rich layer is formed through the deposition of high resistivity material on the surface of a semiconductor substrate, as described by a flowchart for a trap rich layer manufacturing process **900** in FIG. **9**. Upon starting at **901**, the semiconductor substrate is prepared, or partially prepared, (at **902**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The high resistivity trap rich layer material is then deposited (at **903**) onto the surface of the semiconductor substrate. This technique (up to **903**) has been used to form a trap rich layer in some prior art structures, but in some embodiments of the present invention, this technique may be combined (at **904**, before or after **903**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **905** before the process **900** ends at **906**.

The material deposited at **903** may be polycrystalline semiconductor material or polycrystalline silicon (polysilicon) or amorphous silicon. For polysilicon, grain boundaries of polysilicon crystallites within the deposited material generally provide the desired trap states. For amorphous silicon, the silicon atoms generally form a continuous random network (CRN) configuration that provides dangling bonds from point defects, which in turn produces trap states.

A conformal layer of material deposited at **903** can generally be obtained by isotropic deposition methods, such as LPCVD (Low Pressure Chemical Vapor Deposition), APCVD (Atmospheric pressure CVD), PECVD (Plasma-enhanced CVD), HWCVD (Hot Wire CVD) and sputtering, depending on the type of trap rich layer material. A planar layer can generally be obtained by anisotropic/directional methods, such as PECVD, E-beam evaporation and epitaxial-reactor techniques, depending on the type of trap rich layer material. Multiple depositions of materials may also be performed, e.g. repeating the deposition process, for thicker films and multi-layer combinations.

Additionally, in some embodiments using a handle wafer and layer transfer, the entire handle wafer is comprised of the high resistivity polysilicon. In this case, the trap rich layer extends through the entire extent of the handle wafer. Such embodiments would exhibit the advantageous characteristic of excellent performance and low cost because polysilicon wafers are less expensive than monocrystalline silicon wafers

and because the traps would be located throughout the thickness of the entire handle wafer.

In some embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed by a recrystallized polysilicon technique on the surface of a semiconductor substrate, as described by a flowchart for a trap rich layer manufacturing process **1000** in FIG. **10**. Upon starting at **1001**, the semiconductor substrate is prepared, or partially prepared, (at **1002**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. An amorphous silicon layer of material is then deposited (at **1003**) onto the surface of the semiconductor substrate. A rapid thermal anneal (RTA) is then performed (at **1004**) on the top surface of the semiconductor substrate until the amorphous silicon layer becomes polycrystalline. As a result, grain boundaries of polysilicon crystallites within the deposited and annealed material generally provide the desired trap states. Additionally, the amorphous silicon may be deposited (at **1003**) onto the sides and bottom of the semiconductor substrate, but these parts of the amorphous silicon layer may not recrystallize (at **1004**) to the same degree as the surface exposed directly to the radiation of the RTA process.

This technique (up to **1004**) has been used to form a trap rich layer in some prior art structures, but in some embodiments of the present invention, this technique may be combined (at **1005**, before or after **1003** and/or **1004**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1006** before the process **1000** ends at **1007**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through energetic particle damage techniques. These techniques generally project energetic particles towards the semiconductor substrate to create a displacement-damaged area in the semiconductor substrate when the energetic particles collide with the semiconductor material, with or without changing the chemistry of the semiconductor substrate. The trap states are generally produced by the displacement damage. Such techniques generally include irradiation (e.g. using fundamental particles such as electrons, neutrons, or protons or using EM waves or gamma rays, etc.) and implantation of high energy particles/ions (e.g. using a noble gas, Silicon, Oxygen, Carbon, Germanium, etc.) into the semiconductor substrate.

In some cases using particle implantation with layer transfer techniques, the implantation can be done into the handle wafer with or without a bonding layer already present. However, the implantation is generally easier in most cases without the bonding layer, since some materials (e.g. an oxide) for the bonding layer can impede the implantation. On the other hand, if the bonding layer is a thermal oxide material, the heat from the formation of the bonding layer after the implantation for the trap rich layer could degrade the trap rich layer. In this case, the implantation is done after the thermal oxidation. For example, an implantation of Argon through about a 1000 Å thermal oxide could be performed at about 1 E15/cm^2 and about 240 keV energy. The resulting damage in the silicon substrate will generally extend from the silicon surface to a depth of approximately 2000 Å.

The implanted particles could be Argon or Silicon or other suitable ions and the semiconductor substrate could be very lightly doped silicon such that it has high resistivity. Argon could beneficially be employed because it has a relatively large mass, so it will do substantial damage; but it is also inert, so it will not cause any unexpected side effects. Silicon, on the other hand, could be used as the implanted material for similar reasons in that the silicon will disrupt the silicon crystal structure of the handle substrate layer **205**, but it will not have any other side effects. Oxygen or carbon could be beneficially used for implantation because they can form a relatively stable trap density with respect to subsequent thermal annealing due to the formation of Si—O or Si—C bonds, which disrupt the silicon crystal lattice, leaving some Si bonds dangling. In addition, with sufficient dose and subsequent thermal annealing, O atoms may start to coalesce, forming SiO_x precipitates, which will form stable trap sites in the silicon lattice.

Additionally, multiple implants or irradiation steps (e.g. each with different species/particle, energy levels and/or dose) can be used to tune the damage depth and damage gradient (with respect to depth). For example, the dose can also be varied with the energy to create an almost constant trap density vs. depth. As an example of a two-implant sequence that results in an almost constant damage profile vs. depth, an implantation of Argon at 1E15/cm2 and 240 keV can be followed with a second implantation of Argon at 3E14/cm2 and 60 keV. This sequence will generally result in a damage profile that is almost constant from the semiconductor substrate surface to a depth of about 3000 A. Furthermore, the implantation can be done with a low beam current and/or backside wafer cooling to prevent self-annealing of damage due to self-heating from the implant beam.

In some embodiments using radiation, the trap rich layer may be formed throughout the entire semiconductor substrate by irradiating the semiconductor substrate by exposure to relatively high-energy ionizing radiation, such as gamma rays, X-rays or other suitable high-energy particle sources (e.g. MeV electrons, protons or other high-energy particle that can cause semiconductor lattice damage). A suitable gamma ray source, for example, may be Cobalt-60.

An advantage of using some forms of radiation is that it can penetrate easily through the entire semiconductor substrate, thereby forming the traps throughout the entire bulk of the semiconductor substrate. (Implantation, on the other hand, typically penetrates to a much shallower depth into the semiconductor substrate.) This feature makes the trap density per unit volume relatively constant throughout the thickness of the semiconductor substrate and can create a high integrated trap density per unit area of substrate surface, which is desirable. An alternative is to irradiate the surface of the semiconductor substrate with a low-energy radiation that cannot penetrate very deeply into the semiconductor substrate, so only a surface layer of traps is formed.

Another benefit of irradiation is that it can be performed on a semiconductor substrate with almost any type of surface films previously deposited thereon. Therefore, a bonding layer, for example, can already be present at the surface of a handle wafer. Due to the high penetration depth of gamma rays, for example, most of the radiation will pass through the bonding layer and into the substrate layer. This feature allows the trap rich layer to be created after the deposition or thermal growth of the bonding layer. An additional benefit of trap creation after deposition or growth of the bonding layer is that interface traps may be created at the Si—SiOx interface, causing an additional layer of traps at the bonding surface of the semiconductor substrate. Having a layer of traps at this

surface can be beneficial by preventing inversion or accumulation of free carriers at this surface. Another benefit of forming the trap rich layer after thermal oxidation is that thermal oxidation requires high temperatures and long times which can result in annealing and degradation of previously created traps, which is counter to the general goal of high trap density. Also, although the bonding layer could be formed by CVD, in some cases a thermally grown oxide for the bonding layer may have more desirable properties than a CVD oxide.

Another benefit of irradiation for inducing trap formation is that because of the high penetration depth (e.g. of gamma rays), an entire box of semiconductor wafers (typically 25 wafers in a box) can be irradiated as a batch, which saves time and money. Also, the wafer box can be left sealed during the irradiation procedure, since the radiation can penetrate the box, thereby preventing potential contamination of the wafers. This feature also allows exposure to take place in an industrial environment, instead of in a clean room, thereby reducing cost and increasing the number of fabrication places that can be used for the procedure.

The irradiation technique could be used on SOI wafers in addition to bulk semiconductor wafers. However, the top semiconductor layer of the SOI wafer would be damaged too. A rapid top surface annealing could repair some of the damage to the top semiconductor layer. However, such annealing may not be allowable if CMOS processing of the top semiconductor layer has already occurred. On the other hand, if the damage to devices made in the top semiconductor layer was acceptable, then the trap creation could take place after CMOS processing without a subsequent repair anneal. This option could be simpler and less expensive than creating a trap rich layer in an SOI wafer before CMOS processing. Irradiation could also be used in combination with other trap generation mechanisms to cause an overall increase in the effective resistivity. For example, after implantation the semiconductor substrate could then be irradiated.

The projection of energetic particles is typically a highly directional process. Therefore, for the particles to properly hit some surfaces, such as the upper portions of the walls inside holes that extend down into the semiconductor substrate, the particles may have to be projected at an angle (i.e. not perpendicular) to the top surface of the semiconductor substrate in some embodiments. Additionally, the semiconductor substrate may have to be rotated in order for the particles to hit all of the desired surfaces within the holes.

In some embodiments, some energetic particle damage techniques may be combined with other trap rich layer formation techniques described herein in order to enhance or improve trap rich layer structures and/or functions, even within structures similar to those of the prior art. For example, after initial damaging by another technique to form various shapes with additional surfaces or interfaces within a layer of the semiconductor substrate, the semiconductor substrate could then be put through irradiation. The additional surfaces would thus provide various locations at which a greater density of radiation damage may occur.

A flowchart for a trap rich layer manufacturing process **1100** using energetic particle damage is shown in FIG. **11**. Upon starting at **1101**, the semiconductor substrate is prepared, or partially prepared, (at **1102**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. A screening layer is then deposited (at **1103**) onto the surface of the semiconductor substrate. The screening layer is generally an amorphous layer of material that scatters the subsequently projected particles to prevent channeling regardless of the original angle of projection of the particles. The material may be SiO2, amorphous Si or other appropriate material. Additionally, the morphology of the screening layer may be conformal or planar. The particles are then projected (at **1104**) toward the surface of the semiconductor substrate to cause the damage for the trap rich layer. In some embodiments of the present invention, this technique may be combined (at **1105**, before or after **1103** and/or **1104**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1106** before the process **1100** ends at **1107**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through nanocavity formation techniques as described in a flowchart for a trap rich layer manufacturing process **1200** shown in FIG. **12**. Nanocavity formation techniques generally implant helium into a semiconductor substrate. The implanted helium generally congregates together in "bubbles" within the semiconductor substrate at a depth determined by the projected range of the helium into the semiconductor substrate. Dosing helium beyond 1 e16 #/cm2 generally causes the formation of a "band" of the helium bubbles. The helium energy generally determines the depth of the bubble band formation and the dose generally determines the size of the bubbles formed. Application of an anneal step (e.g. at about 1000 C for about 20 minutes) outgasses the helium, leaving behind nanometer-scale cavities representing damage to the crystal lattice.

In the prior art, nanocavity techniques have been investigated for gettering purposes to introduce defects in certain places displaced apart from active surface regions of a semiconductor substrate. Such defects generally pull in impurities, thereby moving the impurities into the defects and away from the active surface region. For trap rich layer purposes, on the other hand, the surfaces of the cavities left behind after outgassing the helium provide the trap states.

Upon starting at **1201**, the semiconductor substrate is prepared, or partially prepared, (at **1202**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. (In the case of an SOI wafer, the implantation of the helium may potentially be performed before or after formation of the buried oxide layer, since the helium ions could penetrate through this layer. Similarly, in the case of a handle wafer, the implantation of the helium may potentially be performed before or after formation of the bonding layer, since the helium ions could penetrate through this layer.) A screening layer is then deposited (at **1203**) onto the surface of the semiconductor substrate. The screening layer is generally an amorphous layer of material that scatters the subsequently projected helium particles to prevent channeling regardless of the original angle of projection of the helium. The material may be SiO2, amorphous Si or other appropriate material. Additionally, the morphology of the screening layer may be conformal or planar.

Helium ions are then projected (at **1204**) toward the surface of the semiconductor substrate to cause the helium bubble formation at the desired depth. Multiple implants (each with different energy and dose) may be performed (at **1204**) to tune the helium accumulation depth and the average helium bubble size. Additionally, a non-perpendicular ion beam angle and rotation of the semiconductor substrate (at **1204**) may allow implantation into vertical surfaces (e.g. sidewalls

of holes and/or trenches) of the semiconductor substrate and assist in preventing channeling.

The semiconductor substrate is then annealed or heated (at **1205**) to outgas most or all of the helium, leaving behind the nanocavities. Since helium is relatively light and is a noble gas, it doesn't adhere to or passivate the cavities or get stuck in the silicon lattice after implantation. Therefore, when it is heated, it merely evaporates out of the semiconductor substrate.

In some embodiments of the present invention, this technique may be combined (at **1206**, before or after **1203**, **1204** and/or **1205**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. (For example, irradiation or ion implantation may be combined particularly well with nanocavity techniques, since the cavities will provide a lot of surface area at which additional interface state damage may be done to increase the total damage.) Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1207** before the process **1200** ends at **1208**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through porous silicon etching techniques as described in a flowchart for a trap rich layer manufacturing process **1300** shown in FIG. **13**. Porous silicon etching techniques generally selectively etch a series of pores into the surface of a semiconductor substrate, typically with an electrochemical etch or anodization process, to form a porous silicon layer (PSL). In the prior art, porous silicon etching techniques are used to form gas sensing devices and texturing for solar cells, among other applications. For trap rich layer applications, dangling bonds at the sidewall surfaces of the pores generally provide the trap states.

Upon starting at **1301**, the semiconductor substrate is prepared, or partially prepared, (at **1302**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The pores are then etched (at **1303**) to form the porous silicon layer. For vertical surfaces, such as the sidewalls of holes or trenches in the semiconductor substrate, an electrolytic etching cell for electrolytically controlled etching (ECE) may be set up to get the pores down into the holes and formed laterally.

If the etch process leaves undesirable material inside the pores, then a treatment process may have to be performed (at **1304**) to remove the remaining material. Additionally, a layer of sealing material is placed (at **1305**) over the pores to ensure that no undesirable material enters the pores during subsequent processing. The sealing material may be an insulator layer or the start of the formation of a buried oxide layer for an SOI wafer or of a bonding layer for a handle wafer. Alternatively, the sealing material may form a smooth surface on which the insulator, buried oxide or bonding layer may be formed.

In some embodiments of the present invention, this technique may be combined (at **1306**, before or after **1303**, **1304** and/or **1305**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. (For example, irradiation or ion implantation may be combined particularly well with porous silicon etching techniques, since the pores will provide a lot of surface area at which additional interface state damage may be done to increase the total damage.) Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1307** before the process **1300** ends at **1308**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through semi-insulating polysilicon (SIPOS) techniques as described in a flowchart for a trap rich layer manufacturing process **1400** shown in FIG. **14**. SIPOS layers can serve as electrically insulating layers as long as any bias across it is too small to generate current flow. SIPOS layers generally consist of silicon crystallites and SiO2 grains surrounded by a matrix of thin sheets of disordered silicon. The interface or surface between both types of crystallites and the matrix generally provides the desired trap states.

Upon starting at **1401**, the semiconductor substrate is prepared, or partially prepared, (at **1402**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The SIPOS material is then deposited (at **1403**) onto the surface of the semiconductor substrate, e.g. by chemical vapor reaction of SiH4 and N2O in an N2 carrier gas through a CVD or LPCVD process. The size of the silicon crystallites may be tuned by varying the deposition temperature and oxygen concentration. Additionally, since the SIPOS material is conformal, it can potentially reach into holes and trenches in the semiconductor substrate.

For an SOI wafer, the buried oxide layer may be formed over the SIPOS layer, e.g. by oxide deposition. The SIPOS layer may have to be smoothed prior to placing the buried oxide material. In some alternative embodiments, since the SIPOS material is semi-insulating, the SIPOS layer may be used as both the trap rich layer and the buried oxide layer, depending on whether the SIPOS layer is sufficiently insulating to serve as the buried oxide layer too.

In some embodiments of the present invention, this technique may be combined (at **1404**, before or after **1403**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1405** before the process **1400** ends at **1406**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through thermal stress relief techniques as described in a flowchart for a trap rich layer manufacturing process **1500** shown in FIG. **15**. Thermal stress generally occurs between two materials having different coefficients of thermal expansion when the materials are significantly heated or cooled. If the stress is high enough, cracks may develop between the two materials. In the prior art, this situation is generally avoided in order to prevent damage to semiconductor devices. However, for trap rich layer purposes, the formation of the cracks causes defects that provide the desired trap states.

Upon starting at **1501**, the semiconductor substrate is prepared (at **1502**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. A thermal stress relief layer is then formed (at **1503**) on or in the semiconductor substrate. The thermal

stress relief layer is generally a binary semiconductor layer, such as SiGe, SiC, etc. Placing the binary semiconductor material (e.g. SiGe) onto a single-element crystalline semiconductor substrate (e.g. a silicon substrate) will form a heterostructure interface at which the single-element and binary semiconductor layers have lattice constants and coefficients of thermal expansion different from each other.

In some embodiments, the thermal stress relief layer may be direct deposited (e.g. by CVD, sputter, MBE, etc.) onto the surface of the semiconductor substrate. In other embodiments, the thermal stress relief layer may be implanted in a process that obtains the thermal stress relief layer by implanting an ion (e.g. Ge) at a high enough dose such that its molar fraction in the target material (e.g. Si) becomes significant (e.g. $Si_{0.9}Ge_{0.1}$). In other embodiments, the thermal stress relief layer may be formed by wafer bonding and substrate removal. Other techniques for forming the thermal stress relief layer may also be used at **1503**.

At **1504** the semiconductor substrate is rapidly heated to a target temperature, e.g. through an annealing process. As the single-element and binary semiconductor layers are rapidly heated, the two materials expand at different rates. At a sufficiently high temperature, the binary semiconductor layer (which is thinner than the substrate) will develop cracks that will relieve the stress caused by thermal expansion. The cracks cause defects or damage in the binary semiconductor layer. The defects provide the desired trap states. Additionally, if the thermal stress relief layer is conformal, it will form down inside holes and trenches, and the heating will create trap states in these regions too.

At **1505** the semiconductor substrate is cooled back to room temperature. In some embodiments, the cooling may be done rapidly in order to potentially exacerbate the defects for additional trap states.

In some embodiments of the present invention, this technique may be combined (at **1506**, before or after **1503**, **1504** and/or **1505**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. (For example, irradiation or ion implantation may be combined particularly well with thermal stress relief techniques, since the energetic particles will increase the total damage.) Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1507** before the process **1500** ends at **1508**.

In some embodiments using an SOI wafer or handle wafer, the buried oxide layer or bonding layer may be deposited on top of the damaged thermal stress relief layer as part of the further processing at **1507**. Alternatively, before the heating at **1504**, an additional layer of material (e.g. polysilicon, etc.) may be placed on top of the thermal stress relief layer. Then after the heating and cooling (at **1504** and **1505**), the additional layer may be thermal oxidized to form the buried oxide. In another alternative, the heating at **1504** is also used to thermal oxidize the additional layer, thereby forming the trap rich layer and the buried oxide layer almost simultaneously.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through chemical etching techniques as described in a flowchart for a trap rich layer manufacturing process **1600** shown in FIG. **16**. Chemical etching the semiconductor substrate (e.g. with fluorinated chemistry, also known as "texturing") tends to damage the semiconductor surface by forming bumps, short-wide pillars, or tall-narrow columns in a non-uniform randomized morphology, which increase the effective surface area. If the semiconductor surface is undamaged and crystalline prior to the chemical etch, then the chemical etch will result in an even surface and minimum realizable surface area. However, if the surface is lightly and randomly damaged first (in a processed called "seeding"), the subsequent chemical etch process will be uneven, resulting in the randomized morphology and increased surface area. This process is used in the prior art for solar cell texturing. However, the etched semiconductor surface will thus have significant unpassivated surface states, which are also trap states, the quantity of which is proportional to the effective surface area.

Upon starting at **1601**, the semiconductor substrate is prepared, or partially prepared, (at **1602**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The seeding process is then performed (at **1603**) to cause some initial damage to the surface of the semiconductor substrate, e.g. by scratching the semiconductor substrate surface or impinging a mechanical force onto the surface to cause a relatively small amount of damage.

The chemical etch is then performed at **1604**. The chemical etch may be a plasma texturing/etch, a reactive ion etch (RIE), a wet chemical etch (e.g with HF/HNO_3), a dry etch, a fluorinated plasma etch (e.g with SF_6/O_2) or other appropriate etch technique.

In some embodiments of the present invention, this technique may be combined (at **1605**, before or after **1603** and/or **1604**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. For example, the chemical etch may be followed by irradiation or particle implantation to increase the density of the damage at the surfaces and interfaces generated by the chemical etch. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1606** before the process **1600** ends at **1607**.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through laser texturing techniques as described in a flowchart for a trap rich layer manufacturing process **1700** shown in FIG. **17**. In such techniques, a laser beam is generally scanned in a serpentine pattern to cover the entire surface of the semiconductor substrate. The techniques generally provide a relatively shallow, short time, high temperature (e.g. about 100 C) heating of the impinged surface. The laser impinging on a semiconductor substrate surface generally causes an extremely high temperature gradient "in-plane" of the semiconductor surface. The highly localized temperature gradient is applied such that it cannot significantly raise the base temperature of the entire semiconductor substrate (i.e. through pulsing techniques). Instead, the laser causes the semiconductor material in the immediate vicinity of the laser to evaporate and/or sublimate, resulting in semiconductor substrate surface ablation and defects/dangling bonds.

Laser texturing is typically used in the prior art for treatments of amorphous layers for photovoltaic applications and in thin film processes to anneal amorphous silicon into polycrystalline for LCD applications or thin film transistor displays. For trap rich layer purposes, however, the defects/dangling bonds serve as the desired trap states.

Upon starting at **1701**, the semiconductor substrate is prepared, or partially prepared, (at **1702**) as an SOI wafer, a

handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The laser is then scanned (at **1703**) across the surface of the semiconductor substrate to generate the damage for the desired trap rich layer. In order to treat vertical surfaces, such as the sidewalls of holes or trenches, the laser may have to be projected at an angle and the semiconductor substrate may have to be rotated at **1703**.

In some embodiments of the present invention, this technique may be combined (at **1704**, before or after **1703**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. For example, laser texturing may serve as the seeding process in a chemical etch, as described above. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1705** before the process **1700** ends at **1706**.

In some embodiments using an SOI wafer, the laser texturing may be performed before the buried oxide is formed on top of the damaged material. Alternatively, if the buried oxide layer is thin enough and transparent enough, then it may be formed before the laser texturing, since the laser may penetrate through the buried oxide layer to heat and damage the semiconductor substrate.

In alternative embodiments, some of the trap rich layers described above (and in the aforementioned related patent application Ser. No. 13/652,240) are formed through mechanical texturing techniques as described in a flowchart for a trap rich layer manufacturing process **1800** shown in FIG. **18**. These techniques generally inflict mechanical damage by a transfer of kinetic force to the surface of the semiconductor surface. In the prior art, mechanical texturing or damage is done for extrinsic gettering purposes. For trap rich layer purposes, however, the damaged areas serve as the trap rich layers.

Upon starting at **1801**, the semiconductor substrate is prepared, or partially prepared, (at **1802**) as an SOI wafer, a handle wafer substrate layer (e.g. before the handle wafer is bonded to a wafer containing a circuit layer) or other appropriate semiconductor substrate structure. The mechanical texturing or damaging technique is then applied (at **1703**) to the surface of the semiconductor substrate to generate the damage for the desired trap rich layer. The damage may be caused by one or more of several methods, such as brushing (e.g. scribing) the surface of the semiconductor substrate with a metal or ceramic brush, impinging small balls of hard material onto (e.g. sandblasting) the surface of the semiconductor substrate or grinding (e.g. with a grinding wheel) or abrading the surface of the semiconductor substrate.

In some embodiments of the present invention, this technique may be combined (at **1804**, before or after **1803**) with other techniques described herein to enable enhanced or improved trap rich layer structures and/or functions, even within structures similar to those of the prior art. For example, mechanical texturing may serve as the seeding process in a chemical etch, as described above. Further processing (e.g. similar to that described above, such as to finish preparing the SOI wafer or handle wafer, to form various active or passive devices therein, to perform various layer transfer techniques, etc.) may then be performed at **1805** before the process **1800** ends at **1806**.

In some embodiments using a handle wafer, the mechanical texturing may be performed before the bonding layer is formed. The bonding layer can then be deposited on the surface of the handle wafer and planarized with chemical mechanical polishing (CMP) to allow proper fusion bonding to the top exposed surface of the semiconductor wafer to which it is being transferred. Alternatively, a liquid adhesive bonding agent can be applied to the surface of the handle wafer, allowing the liquid to smooth out the bonding surface of the handle wafer over the mechanically roughened surface of the handle substrate layer.

Although embodiments of the present invention have been discussed primarily with respect to specific embodiments thereof, other variations are possible. Various configurations of the described system may be used in place of, or in addition to, the configurations presented herein. For example, additional layers of passivation and insulation could be disposed in-between described layers where appropriate. As another example, configurations were described with general reference to silicon substrates but any type of semiconductor material could be used in the place of silicon.

Those skilled in the art will appreciate that the foregoing description is by way of example only, and is not intended to limit the present invention. Nothing in the disclosure should indicate that the present invention is limited to systems that are implemented on a single wafer. Nothing in the disclosure should indicate that the present invention is limited to systems that require a particular form of semiconductor processing or to integrated circuits. In general, any diagrams presented are only intended to indicate one possible configuration, and many variations are possible. Those skilled in the art will also appreciate that methods and systems consistent with the present invention are suitable for use in a wide range of applications encompassing any related to improving the electrical performance of semiconductor structures.

While the specification has been described in detail with respect to specific embodiments of the present invention, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing, may readily conceive of alterations to, variations of, and equivalents to these embodiments. These and other modifications and variations to the present invention may be practiced by those skilled in the art, without departing from the spirit and scope of the present invention, which is more particularly set forth in the appended claims.

What is claimed is:

1. A method comprising:

forming a trap rich layer for an integrated circuit by exposing a first wafer that has a substrate layer to high energy particles or radiation to create a displacement-damaged area in said substrate layer; and

forming a circuit layer for the integrated circuit;

wherein said trap rich layer is between said circuit layer and said substrate layer in said integrated circuit.

2. The method of claim **1**, further comprising:

bonding said first wafer with a semiconductor-on-insulator wafer after forming said trap rich layer;

wherein:

said circuit layer is formed in said semiconductor-on-insulator wafer; and

said first wafer serves as a permanent handle wafer for said circuit layer after said bonding.

3. The method of claim **1**, further comprising:

forming a silicon dioxide bonding layer on a surface of said first wafer before forming said trap rich layer;

bonding said first wafer with a second wafer after forming said trap rich layer using said silicon dioxide bonding layer;

wherein:
said second wafer contains said circuit layer;
said exposing said first wafer to high energy particles comprises implanting said high energy particles in said surface of said substrate layer through said silicon dioxide bonding layer.

4. The method of claim **1**, further comprising:
bonding a handle wafer to a top side of said first wafer;
thinning said substrate layer from a bottom side of said first wafer after bonding said handle wafer to said top side of said first wafer;
wherein:
exposing said first wafer with said substrate layer to high energy particles comprises implanting said high energy particles into a bottom side of said first wafer after thinning said substrate layer; and
said forming said circuit layer is conducted before said bonding of said handle wafer to said top side of said first wafer.

5. The method of claim **1**, wherein said exposing said first wafer to said high energy particles or radiation comprises irradiating an entire bulk of said substrate layer using high energy ionizing radiation.

6. The method of claim **1**, further comprising:
bonding said first wafer with a second wafer after forming said trap rich layer;
wherein:
said circuit layer is formed in said second wafer;
said first wafer serves as a permanent handle wafer for said circuit layer after said bonding; and
said exposing said first wafer to said high energy particles or radiation comprises irradiating said first wafer using high energy ionizing radiation.

7. A method comprising:
forming a trap rich layer for an integrated circuit by exposing a first wafer that has a substrate layer to high energy particles or radiation;
forming a circuit layer for the integrated circuit; and
annealing said first wafer to release a plurality of congregated particles within said substrate layer to form nanocavities within said substrate layer;
wherein:
said trap rich layer is between said circuit layer and said substrate layer in said integrated circuit;
said high energy particles comprise a plurality of helium atoms; and
said plurality of helium atoms form said plurality of congregated particles at a depth determined by energy of said plurality of helium atoms.

8. A method comprising:
forming a circuit layer in a first wafer for an integrated circuit;
providing a second wafer having a substrate layer;
etching a surface of said substrate layer to form a porous etched layer having pores with dangling atomic bonds at respective sidewall surfaces; and
bonding said first wafer to said second wafer such that said porous etched layer is between said circuit layer and said substrate layer;
wherein said porous etched layer forms a trap rich layer.

9. The method of claim **8**, wherein said porous etched layer minimizes parasitic surface conduction of said substrate layer in said integrated circuit.

10. The method of claim **8**, further comprising:
forming a second circuit layer in said second wafer prior to forming said porous etched layer;
bonding a temporary handle wafer to said second wafer; and
thinning said substrate layer to expose said surface of said substrate after bonding said temporary handle wafer to said second wafer;
wherein:
said bonding said first wafer to said second wafer creates a conductive electrical connection from said circuit layer to said second circuit layer using a through silicon via.

11. The method of claim **8**, further comprising:
seeding said surface prior to said etching using the application of mechanical force to increase a surface area of said surface;
wherein said etching is conducted using a chemical etch process.

12. The method of claim **8**, wherein said etching is conducted using an electrolytically controlled etch.

13. The method of claim **8**, further comprising:
subjecting said porous etched layer to high energy particles or radiation to increase a trap density of said porous etched layer.

14. The method of claim **13**, wherein said trap density of said porous etched layer exceeds 10^{11} cm^{-2} eV^{-1} after said subjecting.

15. A method comprising:
forming a trap rich layer for an integrated circuit by mechanical texturing a surface of a substrate layer of a wafer; and
forming a circuit layer for the integrated circuit;
wherein said trap rich layer is between said circuit layer and said substrate layer in said integrated circuit; and
wherein said mechanical texturing is introduced to a surface of said wafer using brushing, abrading, grinding, polishing, or chemical mechanical polishing.

16. The method of claim **15**, further comprising:
forming a semiconductor layer on a surface of said wafer;
heating said wafer; and
cooling said wafer;
wherein said mechanical stress is caused by a difference in a thermal expansion coefficient of said semiconductor layer and said substrate layer.

17. The method of claim **16**, wherein:
said wafer is a semiconductor-on-insulator wafer in said integrated circuit having a buried insulator layer; and
said insulator layer and said trap rich layer are both formed by said heating of said wafer.

18. The method of claim **15**, further comprising:
forming a bonding layer on a surface of said wafer after introducing said mechanical stress;
bonding said wafer to a top surface of a second wafer using said bonding layer;
wherein said circuit layer is formed in said second wafer prior to said bonding.

19. The method of claim **18**, further comprising:
planarizing said bonding layer using a chemical mechanical polish prior to said bonding.

20. The method of claim **18**, wherein said bonding layer is a liquid adhesive bonding agent.

21. A method of forming a semiconductor-on-insulator integrated circuit comprising:
preparing a semiconductor substrate;
forming a circuit layer;
depositing a semi-insulating polysilicon layer on a surface of said substrate; and
forming a circuit layer on said semi-insulating polysilicon layer;

wherein said semi-insulating polysilicon layer serves as a trap rich layer for said circuit layer and is sufficiently insulating that it also serves as a buried insulating layer for said semiconductor-on-insulator integrated circuit.

22. The method of claim **21**, wherein:

said depositing utilizes a chemical vapor reaction of silane and nitrous oxide.

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